GaAs IC Reliability in Plastic Packages

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Introduction:

The expansion of wireless and fiber optic telecommunications applications is driving integrated circuit costs down. To respond to the lower price expectations, manufacturers will need less expensive packaging solutions. To survive in plastic and other non-hermetic packages, GaAs ICs must be rugged and have resistance to humidity. This work describes multiple tests applied to investigate a complete set of environmental stresses of interest when qualifying the reliability of integrated circuits in plastic packages. Plastic package tests during the past six years, on over 1500 GaAs MESFET ICs, will be described.

Purpose:

The intent of this work is to demonstrate the immunity of GaAs IC technology to reliability degradation in plastic packaging. For example: worst-case scenarios are used to show complete immunity to high humidity environments. Additionally, typical package evaluation testing is demonstrated as part of an industry standard set of package-related qualification tests.

Methodology:

Historically, a lot more emphasis has been placed upon GaAs device reliability rather than on the packaging capabilities.[1] However, as GaAs moves into high volume production, packaging costs continue to be one of the largest parts of the overall cost of a finished product. Its not uncommon for packaging and testing costs to be higher than the cost of the GaAs die. Plastic packages bring a few more concerns than the traditional high performance hermetic packages that GaAs ICs were typically found assembled in. For example, plastic devices have the extra reliability concerns of stress, moisture penetration, contamination, and corrosion. A well-balanced reliability evaluation approach will address all the concerns of plastic packaging, as well as, the typical reliability concerns of the technology. The common battery of reliability testing used on plastic devices has been the standard set of tests identified in JEDEC 26A.[2] This specification outlines 4 main groups of testing: electricals, package/process, package/chip, and package design. During five years of testing, TriQuint has focused its investigations onto the primary concern of plastic packaging: moisture.[3] Certainly stress and chip factors are important, but endless tables of "no issue" results doesn't tell the manufacturer or customer anything about the weakest link nor what is likely to be experienced upon implementation. However, for those just considering the prospect of high performance devices in low cost packages some baselines are needed.

Plastic package qualification testing began at TriQuint with JEDEC Standard 26A. Back in the late 1980s, 26A provided the only comprehensive set of tests for plastic testing. The common 85/85 (85°C and 85% relative humidity, with bias) was universally implemented but generally unspecified. Accelerated forms of humidity testing were under investigation, but also not standardized. It was widely known that high power devices could routinely pass 85/85 testing because the internal power dissipation of the device could prevent moisture from penetrating to the die surface, where corrosion would ensue for predominantly aluminum metallized silicon technologies. TriQuint's first plastic package was a custom 20 lead quad gull wing design, and no sockets existed.[4] For these two reasons (power dissipation drying & lack of standard sockets) moisture testing and lifetesting was conducted in an unbiased mode. Otherwise, JEDEC 26A was followed to the letter.[2]

After success with the standard plastic qualification testing, attempts to find more stringent criteria were made. TriQuint conducted the next set of tests using 85/85 (with minimal bias) and HAST (highly accelerated stress testing) in a side-by-side manner.[5] Although some failures could be generated on engineering samples, the production devices were capable of passing this test also. Complimentary thermal excursion tests were also performed to evaluate mechanical stress issues.

Standard test flows were subsequently developed for device qualification, and three have been completed at the time of publication.[6],[7],[8] Special engineering tests have also been conducted to look specifically at the moisture resistance of GaAs devices.

There are two special considerations for GaAs devices in plastic packages. First, the die coating material which is often used, and the second is high temperature lifetesting. Die coat material is common for many circuits when encapsulated. It is used for GaAs devices for two primary reasons: coating maintains a more stable dielectric environment for the die surface and the coating also provides mechanical protection for airbridges during molding and during thermo-mechanical stresses. While the die coat is not necessarily needed to encapsulate GaAs die, it does tend to increase the yield of packaged devices, and reduce the chance of a random reliability failure caused by mechanical damage.[5]

High temperature lifetesting is a concern since GaAs devices are normally subjected to very highly accelerated lifetests. Since primary GaAs failure mechanisms can be easily accelerated by temperature, lifetests are sometimes conducted at temperatures up to 300°C. High temperature testing is not normally conducted in plastic packages because the glass transition temperature of the plastic is usually between 160°C and 180°C. At temperatures significantly above the glass transition temperature, the plastic actually begins to "melt." Continued cycles above the glass transition temperature can cause anomalous failures which would never be observed during actual use. TriQuint characterizes the effect of the glass transition temperature threshold by conducting temperature ramp tests and lifetests at multiple temperatures.

Figure 1. Effect of Plastic on Lifetest Results

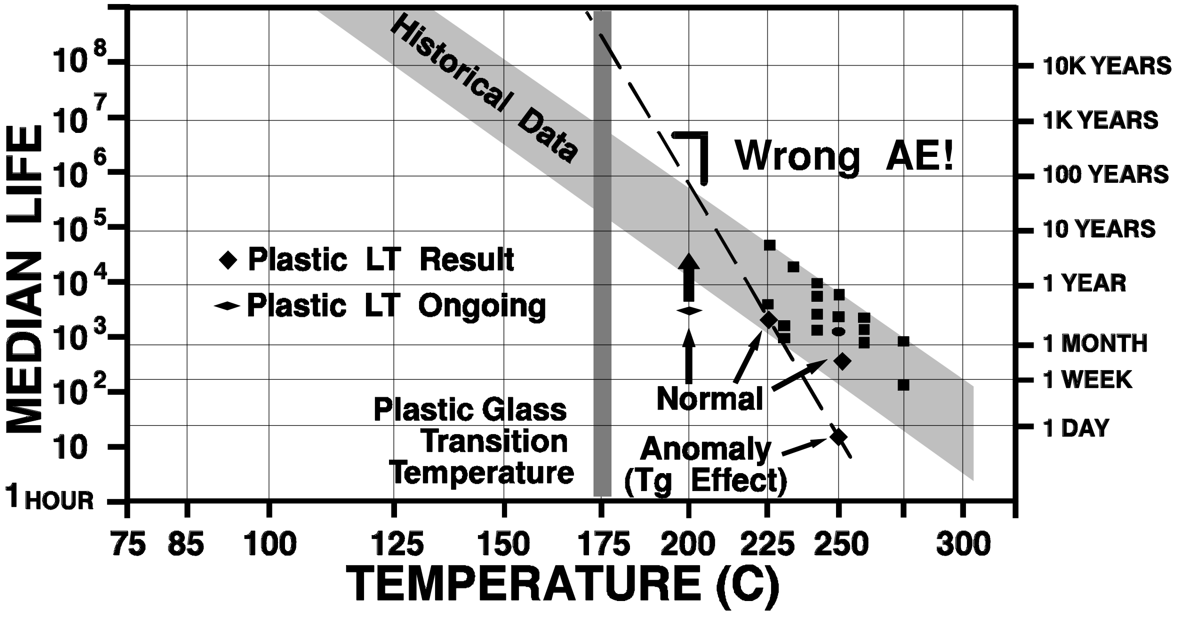

Figure 1 shows the effect of a threshold triggered failure mechanism caused by the glass transition temperature of plastic molding compound. Once the threshold is crossed, the anomalous mechanism can significantly reduce the measured lifetimes, thus indicating an artificially high activation energy and an unrealistic lifetime expectation. The anomalous results are revealed by additional results which are more typical at 200°C (not yet completed - no failures at 3,000 hours), 225°C, and even at 250°C. These results indicate the need for step stress or ramp stress tests to identify the threshold levels.[9] Note that plastic results are similar to all other IC results.

Results:

The central set of testing performed in this study involved the completion of all package-related tests outlined in JEDEC-STD-26A: *General Specifications for Plastic Encapsulated Microcircuits for Use in Rugged Applications*. The tests performed include: physical dimensions, marking permanency, solderability, autoclave, lifetest, humidity test, lead integrity, resistance to soldering heat, thermal shock, and temperature cycling. Both biased and unbiased humidity and lifetesting were performed. To counteract the thermal effect of testing without bias, the lifetest was operated at 150°C ambient, which is 25°C hotter than 125°C ambient stated in the specification. Both the plastic package and the die were therefore exposed to greater temperatures in this unbiased version of the lifetest. This hotter condition is more stringent than biased testing at lower temperatures since GaAs failure mechanisms are primarily accelerated by temperature. In an unbiased humidity test, the moisture is allowed to saturate the plastic and penetrate completely to the die surface. Whereas in a biased test, the heat that is generated on the circuit tends to drive the moisture away. Both life and humidity tests exceeded the minimum specified 1,000 hours with no failures. All standard testing was completed without experiencing a failure. [2]

Table 1. Typical Plastic Package Qualification Requirements				
Requirements defined by JEDEC Standard No. 26-A				
Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications.				
		JEDEC-STD-22		**(rejects allowed)**
Group	**Test Description**	**Method**	**Condition**	**Samples**
	1. Physical Dimensions	B100	Per Data Sheet Package Drawing	2 (0)
	2. Mark Permanency	B107	Resistance To Solvents	4 (0)
B	3. Solderability	B102	25 Leads Minimum Accept Number = 1	3
	4. Autoclave	A102	Unbiased 2 Atmospheres Saturated Steam, +121°C 96 Hours Minimum	100 (1)
C	1. Biased Lifetest	A108	Ambient = 125°C or $T_{peak} << (T_{g} - 5°C)$ 1000 Hours Minimum	77 (1)
	2. Biased Humidity Life	A101	85°C / 85% Relative Humidity, 1000 Hours Minimum	77 (1)
	1. Lead Integrity	B105	25 Leads Minimum Accept Number = 1	3
D	2. Resistance to Soldering Heat	B106	260°C Solder Dip, 10 seconds	22 (0)
	3. Thermal Shock	A106	-40°C to +125°C 100 Cycles Minimum	77 (1)
	4. Temperature Cycle	A104	-40°C to +125°C 1000 Cycles Minimum	77 (1)

Additional tests have been performed to validate good reliability performance in plastic. Accelerated temperatures between 135°C and 260°C have been employed, in plastic. Biased HAST tests at 85% RH and 135°C have also been performed.[5] By successfully completing this series of tests, six separate device/package types have been qualified starting as early as 1990.

Table 2. Device Qualification Requirements

Item	Test Name	Purpose	Condition/Method	Sample Size
1	Thermal Analysis	Temperature Profile Peak Temperature	IR Thermal Imaging Liquid Crystal	1
2	ESD Sensitivity	Damage Threshold	MIL-STD-883, Method 3015	min.9
3	Voltage Ramp	Find Design Limit & Verify Absolute Maximum Rating	Voltage Step Stress in 0.5 Volt Increments at Room Temperature	3 to 5
4	Temperature Ramp	Find Design Limit & Verify Absolute Maximum Rating	Ramp Ambient Temperature to Fixture Failure at Nominal Bias.	3
5	Lifetest	Determine Median Lifetime	Nominal Static Bias Accelerated Temperature.	30 to 100
6	Temperature Cycle	Material Stress and Thermal Mismatch.	1000 Cycles, -40°C to +125°C	77
7	Resistance to Soldering Heat	Test Immunity to Assembly Procedures	Unbiased Test at 300°C for 5 minutes	9

Table 3. Plastic Device Qualification Summary

Item	Part Type	Package Qualification	Device Qualification	Sample Size
1	Multifunction ASIC, 20 pin quad gull wing	Yes		58
2	SPST Switch, 20 pin quad gull wing	Yes	Yes	486
3	Amplifier/Switch ASIC, 24 pin SSOP	Yes	Yes	437
4	800 MHz Amplifier, 8 pin SOIC		Yes	203
5	RFIC Downconverter, 14 pin SOIC		Yes	185
6	Transmit/Receive Amp, 24 pin SSOP		Yes	134

Specific reliability experiments have also been performed to focus on the most critical factor for silicon ICs in plastic, humidity. Two special experiments involving humidity acceleration were performed in cavity packages to represent "worst case" scenarios. Combinations of extra water and extra epoxy (which can outgas water vapor under some conditions) were purposely introduced into package cavities prior to seal. The devices were first cooled to -20°C for about 30 minutes in an unbiased mode. This step was designed to condense all the moisture on the cavity and die surfaces inside the package. Then the devices were powered and forced to 80°C for a 15 minute dwell. The power was removed from the devices and they were frozen again. Twenty-one 132-pin devices were run in this test for 1000 cycles without any failures developing. The samples were measured at interim points of 100, 200, and 500 cycles using a product testing sequence which conducts 129 functional and parametric evaluations. Even under conditions exceeding 200,000 ppm moisture, no anomalous defects or changes were observed.[10],[11] An additional worst case test was designed to specifically evaluate the GaAs technology in humid environments with minimal interactions of any particular package style. A special Technology Characterization Vehicle (TCV) was selected to provide the maximum number of independent active devices, so that various bias conditions could be investigated in humidity. The TCV was packaged in an industry standard Dual In-line Package (DIP) without any lid. The packages were biased while in a test chamber providing an 85°C environment with 85% relative humidity. To reiterate, the die were completely exposed to the high humidity and temperature while biased for the duration of the test. The samples were measured at interim points of 168 and 500 hours using an automated electrical measurement system which conducts 5 key parametric tests. In all, 294 FETs were tested for 1,000 hours. The devices survived, and exhibited less than 1% change in DC parameters.[3] This type of accelerated engineering testing on unprotected dice would not be used on a silicon device because of the expected corrosion on the bond pads and aluminum interconnect layers.

A relatively new test for plastic devices is the "popcorn" test. The popcorn effect is caused when moisture inside a plastic package turns to steam and expands rapidly during vapor phase or infrared solder reflow. Under certain conditions, the force from the expanding moisture can cause stresses inside the package. In the most severe cases, the stress can result in external package cracks. This is commonly referred to as the popcorn phenomenon because the internal stress causes the package to bulge and then crack with an audible "pop." Surface mount devices are more susceptible to this problem because of the soldering methods used and because they have smaller minimum plastic thickness. A group of 20 lead quad gull wing devices were subjected to 72 hours in a pressure cooker at 121°C, 100% humidity, and one atmosphere of overpressure. The group contained samples molded in different molds and with different leadframe finishes. The devices were then run through an IR furnace that heats to a maximum setpoint of 330°C. The devices were then inspected under high magnification, and no cracks were observed.[12] Results are summarized in Table 4.

Table 4. Popcorn Test Details
20 Lead Plastic Quad Gull Wing Package

Sample Size	Mold Type	Lead Condition	Hours in Pressure Cooker	IR Soldering Cycles	Failures
10	Old	Nickel Plated	72	2	0
10	Old	Bare Copper	72	2	0
10	New	Nickel Plated	72	2	0
6	New	Bare Copper	72	2	0
Total Parts = 36			72	2	0

Impact

The results of this work clearly demonstrate acceptable reliability performance of GaAs IC technology in plastic packaging. This not only provides evidence that GaAs devices are ready for low-cost non-hermetic packages, but that GaAs ICs may have superior reliability performance compared to silicon devices, particularly under accelerated humidity conditions.

Table 5. Plastic Package / Humidity Test Summary

Test Description	Plastic or Engineering	Sample Size
Standard Tests	Plastic	1503
Special Humidity Tests	Engineering Mode	351
Totals		1854

Summary

In conclusion, GaAs die have been found to be reliable in plastic package testing. The following points have also been discussed:

1) It is important to conduct various tests that stress the expected failure mechanisms for plastic packages in addition to stressing the die itself.

2) Historical testing over the past five years has indicated that the reliability of GaAs devices in plastic packaging has similar reliability to cavity packaged devices.

3) It is important to characterize the threshold triggered failure mechanisms that affect plastic packages because of low glass transition temperatures.

4) Highly accelerated moisture tests engineered for examining expected plastic failure mechanisms have indicated that GaAs devices have a better immunity to corrosion exhibited by aluminum interconnects used in typical silicon technologies.

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