Thermal Excursion Accelerating Factors

William J. Roesch
TriQuint Semiconductor, Inc., 2300 N.E. Brookwood Parkway, Hillsboro, Oregon 97124-5300
Phone: (503) 615-9292 FAX: (503) 615-8903 EMAIL: billr@tqs.com

Introduction:

For more than a decade, the focus of GaAs reliability testing has been on high temperature life testing. Several failure mechanisms are highly accelerated by temperature, so this methodology has produced data that is easy to analyze and straightforward to predict applicable lifetimes – albeit very long lifetimes. To the contrary, GaAs devices actually fail for quite different failure mechanisms during typical use. This study will address a failure mechanism accelerated by thermal excursions instead of high temperatures. Thermal excursion mechanisms are ones accelerated by temperature cycling, thermal shock, or simulation of infrared (IR) reflow.

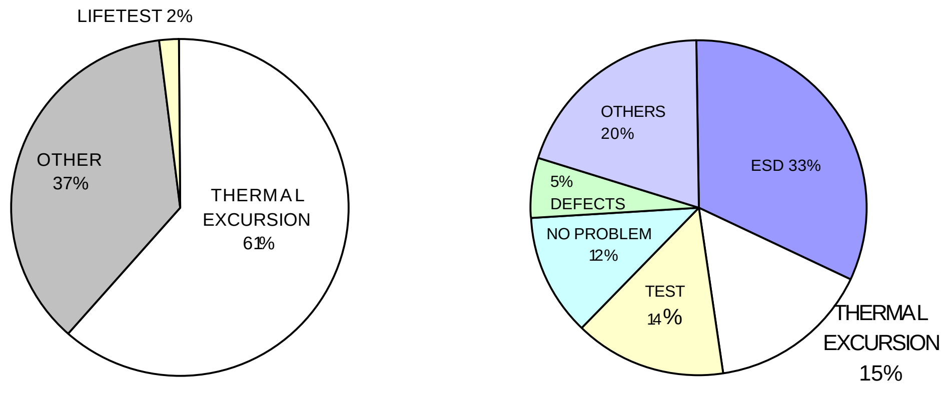
Purpose:

The intent of this work is to provide information on the methodology, implementation, and results of reliability assessments enacted by thermal excursion testing. This project addresses these questions: 1) What is a thermal excursion failure mechanism? 2) What are the factors accelerating thermal excursion failure mechanisms? and 3) How is thermal excursion testing related to what is expected during use?

History:

Thermal excursion testing to industry standard conditions is typically the most severe type of testing. Of all failures generated by qualification and monitoring test types over the past six months at TriQuint, thermal excursion failures are the most prevalent.

Figure 1. Causes of Reliability Test and Field Failures for the Past Six Months.



Reliability Test Failures

Field Returns

From the left pie chart in Figure 1, over 60% of accelerated reliability test failures have been induced by thermal excursion testing (normalized on a percentage basis). This could indicate that the excursion testing is harsh compared to other types of acceleration. However, the field return data in the right pie chart in Figure 1 also shows that the second leading cause of field returns is due to mechanisms induced by thermal excursions. By these two measures, thermal excursion testing is both important, and representative of what causes failure in devices under normal use in the field. Finding exactly how representative is a goal of this investigation.

Methodology:

Thermal excursion testing is accomplished by subjecting samples to temperature extremes. These extremes are generated by thermal conduction in air, immersion in inert liquids, or by infrared radiation. All of the excursion testing is designed to alternate rapidly between the extremes. Each of the three types of excursion testing used in this study is specified by JEDEC specifications (see Table 1). The test conditions are shown in Table 2. For each test, a sample of 100 parts was selected and measured.

Table 1. Standard Thermal Excursion Definitions.

Test	Type	JEDEC	Range	Cycles
1	Infrared Reflow	JESD22-A113-B	+25ºC to +240ºC	<20
2	Thermal Shock	JESD22-A106-A Condition D	-65ºC to +150ºC	<20
3	Thermal Shock	JESD22-A106-A Not specified	-40ºC to +125ºC	<100
4	Temperature Cycle	JESD22-A104-A Condition G	-40ºC to +125ºC	<500
5	Thermal Shock	JESD22-A106-A Condition B	0ºC to +100ºC	<2500

Table 2. Thermal Excursion Profile Data.

Test	Type	Maximum Transfer Time	Minimum Dwell Time	Maximum Time to Temp.
1	Infrared Reflow	~140 seconds	20 seconds	6 minutes
2	Thermal Shock	10 seconds	2 minutes	5 minutes
3	Thermal Shock	10 seconds	2 minutes	5 minutes
4	Temperature Cycle	1 minute	10 minutes	15 minutes
5	Thermal Shock	10 seconds	2 minutes	5 minutes

The test samples for this study were carefully selected. This population of structures is critical – it took fifteen years of searching to find this particular group! The device is a simple RF function block with wide applicability. The samples originated from a production lot that was returned from a customer for low yield after infrared reflow. Over 200 additional lots were screened as a result (representing more than 2.6 million devices). A particularly “bad” type of a population is needed to guarantee failures over a wide range of conditions within a reasonable number of cycles. In contrast, excursion testing of more than 130,500 production devices in the past eight months hasn’t produced a lot like this. Samples for study were selected from the worst performing lot ever investigated. A particular combination of design rules and process variation resulted in a population of material suitable for this type of investigation. This lot had several remarkable characteristics. Production test yield of the lot was nominal, and performance was consistent throughout the population. The lot was composed of 14 wafers, but only 5 of the 14 wafers exhibited reliability anomalies. The other 9 wafers were nominal with regard to aging by thermal excursions. Of particular interest was that the entire anomalous population was affected by the same mechanism. This was not a phenomenon that affected only a portion of the devices. In other words, the anomalous devices were not an infant population but homogenous throughout all samples aged in this group.

Failure Mechanism

The failure mechanism for these special sample devices is a loss of functionality caused by an increase in resistance of certain interconnect pathways – basically, an open circuit. Investigation of the layout characteristics is summarized by the data shown in Table 3. These failures were not related to the active circuit elements, nor to the resistors or capacitors utilized in the design.

Table 3. Interconnect Component Inventory of Special Sample Devices.

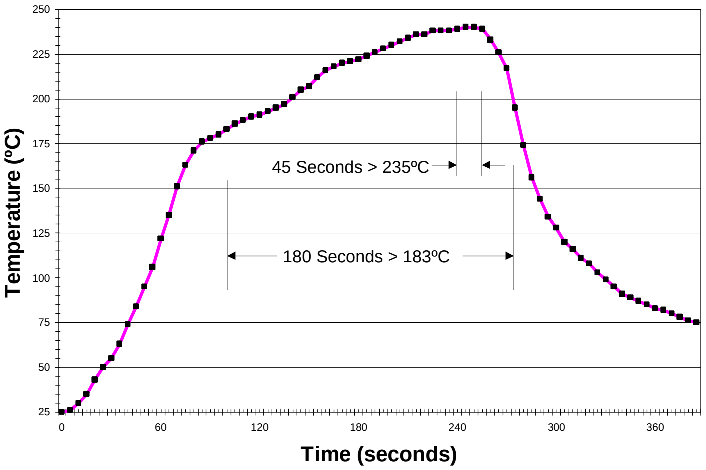
Interconnect Type	Connection	Total	Total Redundant	Total Minimum
1	Metal 1 to Cap Top	17	15	0
2	Metal 2 to Cap Top	1	1	0
3	Metal 0 to Metal 1	30	4	0
4	Metal 2 to Metal 0	2	0	2
5	Metal 2 to Metal 1	2	2	0

The functionality loss for these samples could be easily measured in a DC mode on two pins of the device with respect to ground. During excursion aging, all devices in the population generally experienced increases in resistance. It was also found that currents above 1 mA could “heal” devices, resulting in normal functionality – at least temporarily. Devices were tested at a fixed DC current of 1mA, and a resistance threshold was designated as the failure criteria. This criteria was approximately 2% above the nominal population resistance at time zero. Internal circuit probing determined that the increasing resistance was caused by particular interconnect structures. Electrical isolation and Focused Ion Beam cross-section methods were used to investigate and pinpoint the failure mechanism. Even though this mechanism is quite rare, a layout change and continuous process improvements within the metallization system have further mitigated it.

Results:

Initial testing began with infrared (IR) thermal excursions. The IR thermal profile is shown below in Figure 2. This stress was engineered to simulate the soldering temperatures normally experienced by samples during attachment to the printed circuit board. Most customers will expose parts to this excursion once, and at most twice.

Figure 2. IR Reflow Thermal Profile.

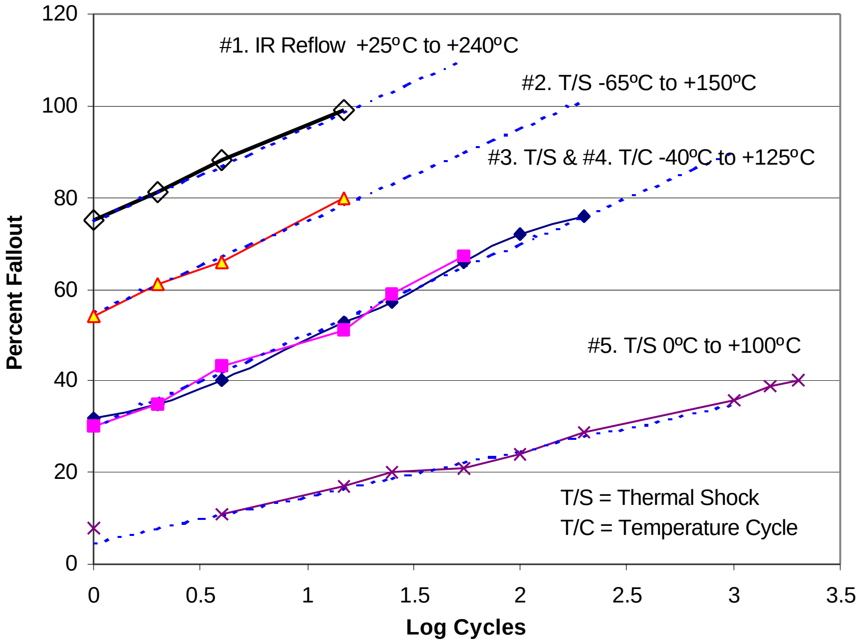


Next, samples were submitted to thermal shock. This type of test is conducted in a “liquid-to-liquid” environment, with a fast thermal excursion between two fluorinert liquid baths – one hot, one cold. The third type of testing used was temperature cycling, which involved air-to-air transfer of material between adjacent chambers at the two temperature extremes.

Failure Distributions.

The resulting failure distributions were analyzed and found to be logarithmic (not necessarily lognormal). In other words, the number of failures increased linearly with the log of the number of cycles (see Figure 3 and equation 1).

Figure 3. Data – Failure Distributions. Regression shown by dashed lines.



Additionally, all of the excursion testing resulted in the same slope of failure accumulation except the most benign test, which had a slope half of the others. This difference would indicate either a "threshold" of some type in the mechanism, or perhaps a different mechanism. When using the same temperature range, both the thermal shock and thermal cycling testing had the same results. Even though the delta (215ºC) of temperatures in an infrared solder reflow (+25ºC to +240ºC) is the same as –65ºC to +150ºC, the IR caused considerably more failures in the same number of excursions.

(failure percentage) = [log (# of excursions) x (*slope)] + constant **<equation 1>**

*slope = 20 for Test #1, #2, #3 and #4 and Slope = 10 for Test #5

<u>Acceleration Factors.</u>

The data indicates that the excursion delta is definitely an acceleration factor for the mechanism in this study. The percentage of initial failures after one cycle at several test conditions is shown in Figure 4. Although this relationship is fairly linear with the three available points, extrapolation is dubious since there are constraints at zero and 100 percent. Because of the slope change in failure distributions at low delta, it is likely that the acceleration also changes. There appears to be another factor besides excursion delta since IR reflow is much harsher than cycling or shock tests.

Discussion:

For the failure mechanism in this study, there is no difference between thermal shock and temperature cycling, at least at the conditions of –40ºC to +125ºC. All five of the tests were logarithmically distributed with coefficients of determination (r-squared) ranging from 0.981 to 0.996. The failure distribution data is remarkably consistent for 4 out of the five tests reported. Four of the tests had a slope of 20% failure per log cycle, and the fifth had a 10%/log cycle slope. However, because of the change in slope, prediction to nominal use conditions would be speculative. It is clear from Figure 3 that for this particular failure mechanism, one IR reflow simulation is approximately equal to 8 thermal shocks from –65ºC to +150ºC, to 144 thermal shocks (or temperature cycles) from –40ºC to +125ºC, and to 4,989,000 thermal shocks from 0ºC to +100ºC. This acceleration shows why such a bad lot is needed to perform this excursion type of acceleration factor testing. Had the samples not failed at a 20% per cycle rate under higher stress, there would not have been any failures to analyze at the low acceleration conditions!

Figure 4. Comparison of Excursion Delta to Failure Percentage after one excursion for Cycling & Shock.

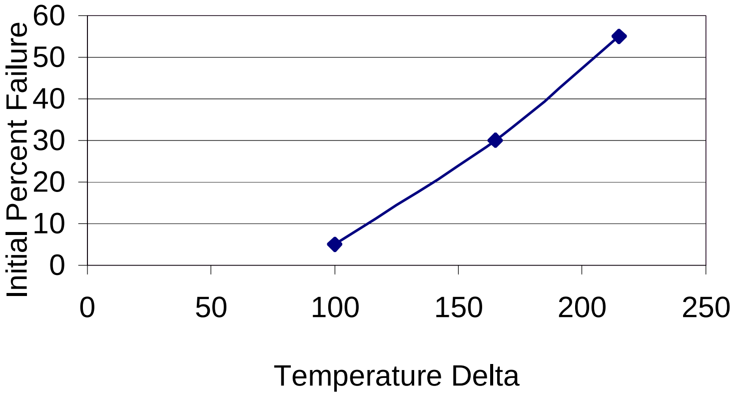


Table 4. Equivalency by Failure Rate between Excursion Tests.

	Test 2	Test 3	Test 4	Test 5
One cycle in Test 1 equals	8 cycles	144 cycles	144 cycles	4,989,000 cycles
One cycle in Test 2 equals	-	17 cycles	17 cycles	70,600 cycles
One cycle in Test 3 equals	-	-	-	260 cycles
One cycle in Test 4 equals	-	-	-	260 cycles

Conclusions:

Each of the following conclusions applies to the failure mechanism present in this special population:

1. Failures in excursion testing are distributed logarithmically.
2. Thermal Shock and Temperature Cycle are equivalent at excursions from –40ºC to +125ºC.
3. As the excursion delta temperatures decrease, the failure rates decrease non-linearly.
4. Infrared reflow excursions are more severe than shock and cycle excursions. For example, one reflow from +25ºC to +240ºC is equivalent to almost 5 million thermal shocks from 0ºC to +100ºC.

Summary:

Application problems and random and infant failure mechanisms predominantly cause field failures. Wearout mechanisms are relatively rare. This work shows that thermal excursion failure mechanisms exist as part of the predominant causes, and that those mechanisms can be characterized. In-depth characterization of these mechanisms leads to acceleration factors that could be used to predict lifetimes under normal use conditions. Understanding these acceleration factors helps us to make correlations of accelerated tests to actual use conditions and to design appropriate testing.

Acknowledgements:

I would like to thank the management at TriQuint for allowing me to submit and present this paper which discloses information on actual failure mechanisms experienced in real-life situations. I would also like to acknowledge Steve Brockett for his failure analysis work in discovering this failure mechanism and Tony Rubalcava for his assistance in analyzing multiple failures generated in this study.