Process Reliability Qualification Experiences During a Fab Relocation

William J. Roesch, Susan Bumgarner, Lita O. Monaghan,
Tony Rubalcava, Denise Riley, Donna Cruse, Jim Cartwright.

TriQuint Semiconductor, Inc., 2300 N.E. Brookwood Parkway, Hillsboro, Oregon 97124-5300
Phone: (503) 615-9292 FAX: (503) 615-8903 EMAIL: billr@tqs.com

Introduction:

The gallium arsenide integrated circuits manufacturing operations in Oregon were recently moved from Beaverton to Hillsboro. A key part of the move involved reliability qualification of the new facility under the time pressure of a fixed move date.

Purpose:

The intent of this work is to provide information on the methodology, implementation, and results of reliability assessments enacted as part of new facility qualification. This project addresses questions of: 1) What aging is required to qualify several processes under a strict deadline? 2) What criteria should be applied to measure success? and 3) What lessons were learned from going through the process?

Methodology:

First, a strategy was developed for the overall facility move. This strategy involved two major phases. The first phase was to "bring up" the new facility and get all equipment functioning, new people hired and trained, and processing started as a totally separate Fab. The second phase was the "shut down" of the original facility with equipment transfer and integration into the new Fab.

Once the overall move plan was in place, the reliability test specifics were discussed. It was decided early-on that a thorough process baseline would be necessary. The baseline included fingerprinting the existing processes. Recipes were compared to ensure that mistakes did not occur in procedures. Individual process steps were characterized to ensure that the process could be produced in the new facility with all relevant film qualities, features, structures, and topography. Additionally, it was decided that analyses would be easier if the process was broken down into smaller groupings, called modules. Visual cataloging and construction examinations were done to define how a wafer should look at each stage of the process flow. Physical checks could then be made to ensure that the process was mimicked.

The critical goal was simple duplication - keep it the same. However, the new equipment differences caused some diversions, and margin improvement was attempted on some parameters (a normal tendency for engineers).

Qualification was approached as a multi-part sequence. In Part 1, the facility was qualified. This meant that the laminar air flow had to have capability to achieve particle specifications. Then the bulk gas was certified at point of use for both particulates and impurities. Lastly, the specialty gasses were piped and certified at point of use for both particulates and impurities.

Part 2 involved verification by Process Engineering. This verification involved the fingerprint, short loop definitions, constructional analyses, and focus on marginal areas. Individual equipment releases were similar to maintenance release practices.

Part 3 was the beginning of structure aging by Reliability Engineering. Both elements and device physical parameters were evaluated for meeting the specification and comparison to the previous facility. Products were checked for compliance and comparison to product in the previous facility. Tests were selected to cover primary concerns of high temperatures, humidity effects, and the thermo-mechanical effects of temperature cycling.

The reliability examinations were planned for three types of processing variations. These were: "*Short Loop*" to look at specific process modules and variables.

"*Hybrid*" to look at single variables in context of full processing. "*Full-up*" to look at one production line vs. the other, start to finish. The tests were developed for two groups of structures: high runner products and qualification elements. The focus areas were developed by a process of identifying and discussing all known failure mechanisms. Each was examined and ranked. The list started with over 150 different failure mechanism concerns. This list was ranked by folks from design, processing, and reliability. The list was reduced down to thirty-five and then finally condensed to ten key concerns.

The ten concerns encompassed previously identified failure mechanisms (from reliability tests and field failures), expected changes from the old Fab to the new Fab, new (and largely unknown) concerns regarding new processes, and other issues of similarity between the Fabs. Other concerns were not necessarily precluded.

Using the list of concerns, the appropriate tests were identified. Because of the deadline for the move, aging conditions were selected to give the quickest possible indications. Our most common accelerants of High Temperature, Moisture, and Thermal Excursions were selected as the three main methods of aging. Additional biased tests were planned for circuits and specific elements.

A key part of the reliability qualification was the development of reliability test structures. The design was configured to cover the mechanisms of concern in the time allowed, and to provide a vehicle for future testing, comparisons, and accumulation of longer term data. One time-saving design application was to make all the test structures wafer probeable with the standard process monitor probe card. On-wafer tests were key to meeting the schedule. Assembly, aging, and biased lifetesting could be conducted in parallel and across the phases of the move plan.

The primary goal of reliability test was comparative data: new Fab vs. old Fab, in terms of the degradation that could be caused by various types of accelerated testing. The secondary goal was overall compliance to the corporate standard.

On top of the facility move, two main new processes needed to be qualified. Additional ancillary testing was added to qualify other new processes by similarity - also during the move.

To cover the primary processes, three new mask sets were designed. After preliminary baseline testing, specific tests and structures were selected for analysis and tracking. Over 1800 discrete electrical measurements were used to evaluate the element structures of interest on each tile. Fabrication of the test wafers started at the end of 1996, and has continued through present day. Over 650 element test wafers have been produced, and approximately 100 are currently in process.

Since some failure mechanisms are accelerated by bias conditions, special fixturing was developed for the element structures. As phase one of the move started, short loop and hybrid runs were started and staged at key points of the process. These wafers were not particularly useful since the initial run was produced with good results, and subsequent runs were all examined on a full-up status.

Stress methodology for elements was refined early on baseline runs. High temperature (275ºC) testing, temperature cycling, and autoclaving of whole wafers needed to be optimized and examined to ensure that anomalous failure mechanisms were not being introduced. The selection of 275ºC was necessitated since previous historical wafer testing had been performed at 250ºC, but it took approximately 12 weeks to cause 20% degradation in FETs. Product testing was performed using the autoclave and temperature cycling, with the addition of biased lifetesting. Several other tests were also performed on a sample basis for information only.

Failure criteria for circuits was simply compliance to the standard production test limits. If actual degradation could not be monitored, then appropriate guardbands were added to the test limits. For example, if RF devices were not serialized or datalogged before testing, the failure criteria was set as a 1dB shift outside the production test limits on critical parameters (gain, for example). Limits for elements were more difficult to set without baseline data. Once preliminary baseline material had been analyzed, it became apparent that changes larger than one order of magnitude were necessary to be "significant" for most parameters. FET shifts were assessed based upon a 20% change criteria, which has been historically utilized. Yield information was interesting, but not generally used as an absolute criterion for qualification testing. The yield data was a good indicator to identify areas for improvement and to assess experimental material quickly, particularly for capacitor dielectrics and via continuity improvements. These type of indicators were not possible on products without detailed failure analysis.

Table 1. Test Identifications.

Elements.

Sample Size: 1 wafer per stress, 3 lots total.

Stress	Condition	Duration
Autoclave	121ºC, Steam, +1Atm.	96 hours
Temp. Cycle	-40ºC to +125ºC	500 cycles
Bake	275ºC (air)	168 hours

Extra: One lot minimum to verify electromigration and bias effects on interconnects, FETs, resistors, and capacitors:

Biased Lifetest	150ºC	1000 hours

Products.

Sample Size: 45 (0 fail) or 77 (1 fail), LTPD = 5, 3 lots.
Note plastic package products include preconditioning.

Stress	Condition	Duration
Autoclave	121ºC, Steam, +1Atm.	96 hours
Temp. Cycle	-40ºC to +125ºC	1000 cycles
Thermal Shock	-40ºC to +125ºC	100 cycles
Lifetest (HTOL)	150ºC	1000 hours

Extra: (for information only)

Bake	150ºC (air)	1000 hours
HAST	85% RH, 135ºC, Bias	50 hours

Results:

Reasonable success in testing was achieved. Conditional qualification of the elements was completed before the second phase of the move. Several of the initial lead product tests were also partially completed before Phase 2 started. With these conditional test completions, there was high confidence that material from the new Fab would pass all testing. The move proceeded on schedule.

Structures. One of the biggest successes of the Fab move qualification, was the design of three mask sets used for reliability investigations. These three designs covered all five processes by similarity. The special reliability test structures were found to be capable of detecting all expected wearout mechanisms and identifying several key yield inhibitors. In this manner, this kind of element mask set can be used for new process development experiments to improve both yield and reliability. Over 1800 unique electrical measurements were made on each of the 20+ tiles per wafer.

Table 2. Reliability Masks Sets

Name	# of Tiles	Processes
4096	26	TQTRx (TQHiP, HA2)
4193	21	QEDA2 (TQHIP, HA2)
4194	26	QEDA, G4 (TQHIP, HA2)

QEDA. The QEDA process was the workhorse process at TriQuint for nearly a decade. It was selected as the primary qualification vehicle because of previous history and its relative simplicity compared to the new processes. Element qualification lots were produced in both Fabs, and samples completed on-wafer testing uneventfully. The lead product selected for qualification was a Dual LNA Downconverter (TQ9203). It was the highest volume product at TriQuint during the Fab relocation. Several lessons were learned during re-qualification of the TQ9203. First, it was noted that some of the planned process "improvements" actually turned out to be detriments and were promptly rescinded. There were also some difficulties encountered with the assembly of the device. A new subcontractor was on trial, and problems with wire bonding resulted. Once the process and package problems were corrected, the part had no other issues, except in autoclave. A particular design sensitivity was uncovered, but not in time (or in magnitude) to allow for a correction during the qualification. This particular quirk was noticed in the previous qualification, but root cause was determined as a result of this process qualification testing. In spite of a few minor setbacks, the new process facility produced devices which compared very favorably with previous generations and those performed on a real-time side-by-side basis.

Pre-Print of a Paper Presented at the 1998 GaAs REL Workshop, November 1, 1998, Atlanta Georgia

TQTRx. The next process qualified was the TQTRx process. In addition to the Fab qualification, this process had an added challenge of being previously unqualified. A converted TQ9203 (Dual LNA Downconverter) product was selected for qualification. Additionally, a TQ9147 power amplifier was selected as a qualification vehicle. Both devices and the element qualification performed well. These devices and elements showed that the new Fab was more than capable of duplicating the reliability of the old Fab - new processes could be successfully run in the new Fab as well.

QEDA2. The third full process qualification testing was completed on another new process - QEDA2. The QEDA2 process is the most complex currently run in the Oregon facility. RF and Digital products were selected for qualification testing. Several anomalies were encountered during qualification testing. These have been addressed in turn, and the result has been a satisfying process evolution which has produced devices capable of passing all tests. Some issues remain with particular new packaging/subcontractors, but the process has improved throughout the qualification process, and has benefited from results achieved during the Fab relocation.

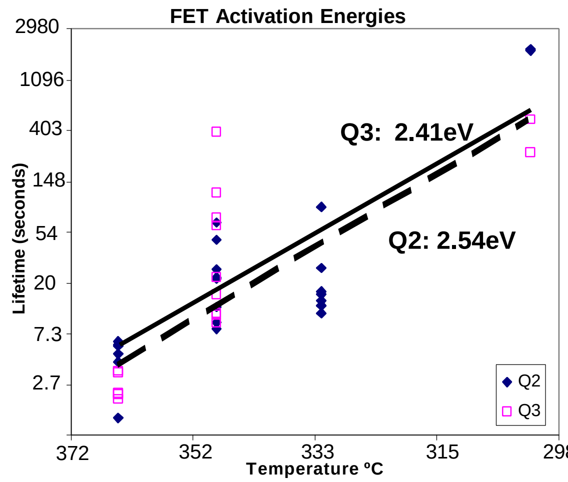
Table 3. Process Improvements

Issue	Correction
Via Chain Integrity	Physical Rule Modifications
Ohmic Metal Attack	Changed Ohmic Overlap
Metal Bridging	Process Enhancement
Incomplete Vias	Via Etch Improvement
Nitride Cracking	Modify Cures and Nitride
Nitride Performance	Revert to Original Recipe
Visual Appearance	Maturity in new Fab

Future Ramifications. As an outcome of the process qualification testing, a program was instituted to conduct process monitoring. The monitor program repeats element tests conducted on wafer. Each calendar quarter, the qualification test slate is applied to evaluate the reliability performance. Fast test methodology has been applied in addition to the unbiased wafer level testing. The traditional and fast test methods have shown reasonable process stability over the investigation period. Two recent results on highly accelerated tests are shown in Fig. 1.

The data indicates very similar lifetimes, with a slight improvement from quarter to quarter. Activation energies were also found to be quite similar even though they were determined by a just a couple of wafers in each quarter.

Figure 1. Fast-Test Process Monitor Results.



Conclusions:

Three major processes were qualified using millions of element & thousands of lead product results.

A qualification methodology has been described which involves use of elements and products. Experience has shown that elemental tests are beneficial in precisely identifying failure mechanisms and the associated process capability. It was also shown here that tests on wafers could provide similar results to packaged products, except that they can yield results in much shorter times. The timeline was particularly important for this Fab move because of the compressed time schedule. The success of this work indicates that a methodology involving elements and circuits through similar stresses is appropriate to evaluate integrated circuit reliability for qualification testing and for continuous process capability monitoring.

Acknowledgments:

The authors would like to thank Process and Product Engineering for their support of the qualification activities described in this paper.