Burn-in of GaAs ICs

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Introduction

To burn-in or not to burn-in has been a topic of growing concern for integrated circuit manufacturers and the companies who use semiconductors in their systems. The silicon fabricators have mounted an impressive case against burn-in recently. The momentum has carried into the military arena with the new QML specification (MIL-I-38535) opening the door for tests that are based on data rather than a cookbook approach that guarantees a minimum quality level and virtually assures nothing better. In the midst of this controversy enters gallium arsenide. Although new and "scary" to a reliability engineer, the evidence is even more convincing that burn-in offers nothing to improve baseline reliability and may even be detrimental to device quality and lifetimes.

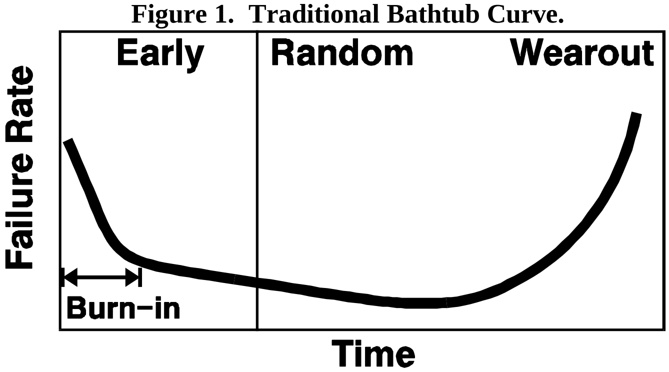
This short discussion offers data in the following four areas indicating why burn-in should not be performed on GaAs ICs:

1. GaAs devices have no early failures.
2. GaAs failure mechanisms are different from silicon.
3. Burn-in reduces GaAs lifetimes.
4. Burn-in reduces GaAs quality.

What is Burn-in?

Burn-in is a screening test designed to remove early or infant failures. The basis of this testing is the "traditional" bathtub curve shown in Figure 1, which suggests that circuits have a high failure rate early in their life. This initial premise is under attack for silicon devices, which are regularly demonstrating defect rates below 100 PPM. Although there once was an obvious need for a method to remove early failures in silicon devices, it should be noted that it has been more than 20 years since MIL-STD-883 was first written, and devices are much more reliable today.

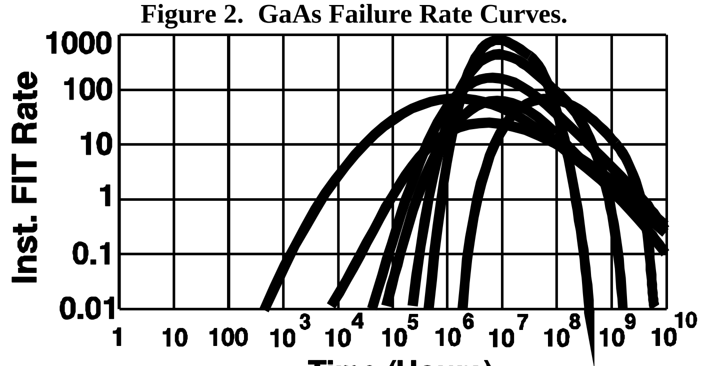
Figure 1. Traditional Bathtub Curve.



For gallium arsenide devices, the likelihood of early failures is even more remote. First of all, there is no historical basis to overcome - GaAs ICs have never exhibited early high failure rates. The data that is available supports a lack of early failures. For example, in burn-in experiments at TriQuint, over 5000 devices were subjected to the standard 168 hour, 150°C burn-in conditions and less than 0.03% of the devices failed for reasons that could be interpreted as early failures.

Additionally, the entire history of field failure analysis has only discovered one device that could be considered an early failure. This lone failure was caused by a processing defect resulting in bridged metal, which could have been screened best by increasing meticulous visual inspection. Assuming this defect level is representative, only a rate as high as 0.01% could be expected. Even lower expected failure rates have been established by lifetesting. Over 300 lifetests have been performed without a single early failure occurrence in a cumulative population of more than 9,300 test structures. This data ensures a best estimate early failure occurrence rate of less than 0.001% (10 PPM). But the most convincing data are the distributions of the wearout failures that eventually were generated at higher stress levels during accelerated lifetesting. These distributions indicate that the bathtub curve probably does not exist for gallium arsenide (see Figure 2). FIT = failures per billion hours.

Figure 2. GaAs Failure Rate Curves.



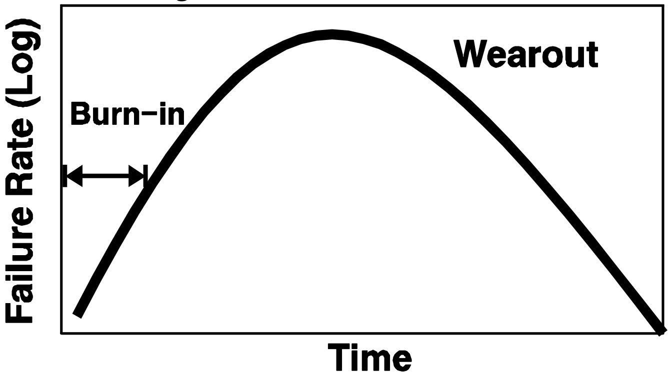
Different Mechanisms

The lack of early failures for GaAs devices is expected from the differences in failure mechanisms. Silicon MOS devices are prone to failures because of oxide defects and time dependant dielectric breakdown in the gate structure. Additionally, all silicon devices are susceptible to various forms of ionic contamination, which are manifested by junction leakage or threshold shifting. GaAs MESFETs are immune to these two mechanisms for which burn-in was specifically designed. GaAs devices are also much less susceptible to electromigration, corrosion, and intermetallic problems which might be caught by a burn-in since gold metallization is utilized instead of the aluminum that is used in silicon ICs.

Reliability Reduction

But the lack of infant failures and difference in failure mechanisms might not be enough to buck the tradition of burn-in. After all, what harm could a little extra screening do? The answer is: "more harm than you might think!" For example consider the failure rate curve in Figure 3. Instead of reducing failure rates with burn-in, devices will emerge from the screen with higher failure rates than when they started. Even though wearout is usually not a concern early in life, demands for sub-FIT failure rates may eventually make wearout a consideration.

Figure 3. GaAs "Bathtub" Curve.



Quality Penalty

In addition to reducing available circuit lifetimes, burn-in almost doubles the opportunity to make a handling mistake and actually cause a defect. The fixturing for high frequency GaAs devices is still immature. GaAs device volumes are relatively small. Both of these facts add up to complex socketing schemes and manual device handling procedures for GaAs circuits. Every handling operation decreases device quality, as shown in Figure 4. Instead of three handling operations to move a part from final assembly to the customer, a burned-in device takes seven handling maneuvers. Those extra steps not only increase the chance of malforming the delicate leads of most GaAs devices, but also increases the risk of causing ElectroStatic Discharge that could damage a device. To emphasize the point about damaged leads, consider Figure 5. The main reason for device returns at TriQuint is for mechanical damage involving bent or malformed leads.

Figure 4. Quality Cost of Burn-in.

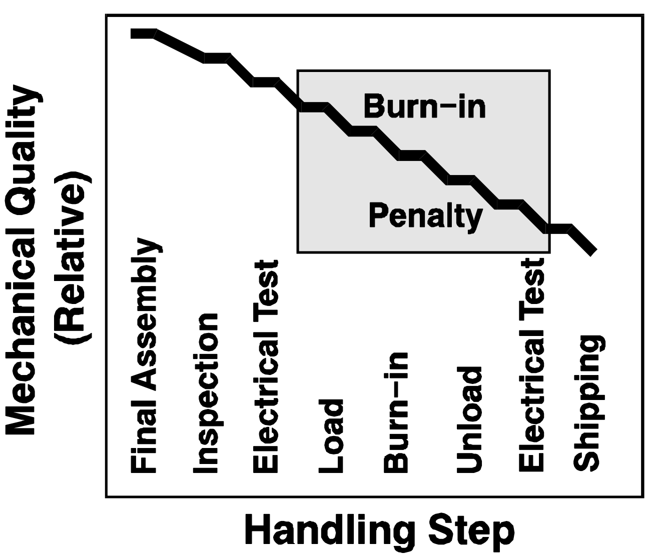
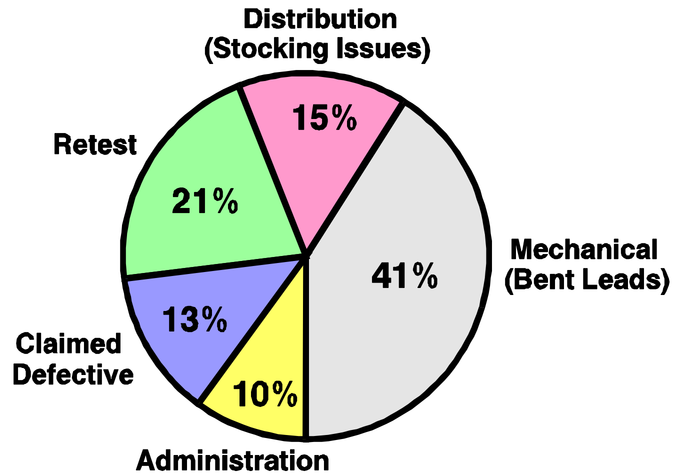


Figure 5. Reasons for Field Returns.



Screen At Any Cost

For most applications, the four-point argument against burn-in is adequate. But there are a few applications where reliability demands are such that not a single failure can be tolerated, regardless of how unlikely it might be or how much must be spent to detect it. For those applications, the answer is still not traditional burn-in. As we've shown, that approach degrades reliability. Instead, other screening techniques need to be investigated. One option might be increased electrical testing with wider guardbands or increased temperature ranges. While ruled-out for traditional applications because it often degrades yield unnecessarily and increases cost significantly, the yield-loss might be tolerated for a high-reliability use. Other options might include increased screening at the board and system levels or alternate stressing techniques that don't increase handling risks.

Conclusion

In this discussion, it's been shown that traditional burn-in offers no benefits in terms of GaAs device reliability. Although burn-in is also becoming less useful for silicon devices, GaAs circuits are different in that there is no historical precedent for performing a burn-in screen. The data base gathered thus far shows no indication of early failures, and the GaAs failure mechanisms which have been characterized are different than the ones for silicon which generated the need for burn-in many years ago. It's also been shown that burn-in is actually detrimental to GaAs device reliability since more handling steps are required to implement it and because it increases the failure rates and uses-up lifetimes expected for GaAs devices. In special applications, alternatives for burn-in may need to be investigated, but GaAs devices have already proven reliability levels exceeding most system requirements.

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