

High-Isolation Low-Loss SP7T pHEMT Switch Suitable for Antenna Switch Modules

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Abstract — In this paper the design, fabrication and measurement of a high performance SP7T GaAs pHEMT switch for cellular phone applications is discussed. The antenna switch design uses a state of the art E/D-mode pHEMT process with an Ron*Coff Figure of Merit of 145 Ohm-fF. Excellent broadband insertion loss measurements across all cellular bands are less than 0.5dB, isolations are greater than 32dB while maintaining minimum harmonic distortion levels. Matching the switch to specific bands yielded insertion losses of 0.35dB at 0.915 GHz and 0.4dB at 1.95 GHz.

I. INTRODUCTION

There are huge demands in place on semiconductor designers and technologists to deliver state of the art components to the cell phone industry. In some cases, a mere 0.1 ohm*mm difference in on resistance of the FET can often be the decisive parameter enabling a company to sell millions of switch modules.

The typical technology employed for the RF switch function in an antenna switch module (ASM) has recently been manufactured in GaAs pHEMT. Historically, these devices have been manufactured at the 0.5 um technology node [1]-[3]. Recently, switches produced on Silicon-on-Sapphire (SOS) or Silicon-on-Insulator (SOI) technology have been developed and are showing improving performance [4], [5].

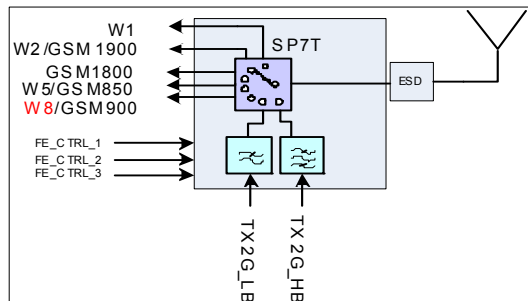


Fig. 1 Block Diagram of an ASM Module using a 7 throw switch with 5 linear throws and 2 Tx paths.

A common ASM can incorporate a switch, two transmit filters and ESD protection all confined in a small 3mm x 3.8mm package. A block diagram of such an ASM is shown in Fig. 1. This paper will detail the manufacture and design of a single-pole seven-throw (SP7T) switch used in an ASM product. Additionally, performance data will be included at the device and module level.

II. PROCESS DESCRIPTION

The devices reported in this paper were fabricated on a 0.25 um / 0.35 um D/E mode process produced on TriQuint's high-volume, 150mm production line. This process consists of dual-recessed AlGaAs/InGaAs pHEMT transistors. The gate is formed through an optical I-line stepper and sidewall spacer process and utilizes a high-reliability refractory gate metal. A cartoon cross-section is shown in Fig. 2 where the FET topology can be seen.

The processing details were reported in [6] and will not be repeated in detail herein. However, this work will feature recent improvements to the process which will be discussed. The typical DC and RF specifications are listed in Table 1.

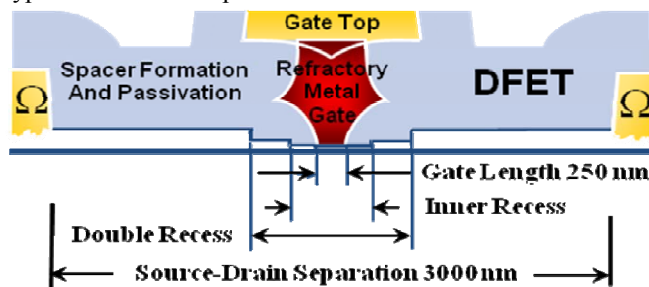


Fig. 2 Cartoon cross-section of a DFET used in the switch core reported in this paper.

Process highlights enabling the performance of the SP7T switch presented here revolve around the transistor topology. First, a 0.25 um DFET process was developed with aggressive Layout Design Rules (LDR) in mind, thus enabling a 2.4 um

minimum ohmic contact width. This narrow ohmic allows a 5.4 μm gate to gate pitch, which proves both beneficial to on resistance and minimizes the FET cell size. The compactness of the transistor still yields a competitive off capacitance. In fact, a common switch Figure of Merit is the product of on-resistance and off-capacitance ($R_{on} \cdot C_{off}$). For the process used, the figure of merit is 145 $\text{Ohm} \cdot \text{fF}$ (or equivalent units of 145 f-sec). This $R_{on} \cdot C_{off}$ performance is believed to be the lowest reported from any GaAs technology, 225 $\text{ohm} \cdot \text{fF}$ [2] and is lower than any reported SOS or SOI technologies of 448 $\text{ohm} \cdot \text{fF}$ and 280 $\text{ohm} \cdot \text{fF}$, reported in [4] and [5] respectively.

Additionally, the switch process includes a very capable 0.35 μm EFET which can be used to build logic and add decoder functionality on chip. Coupled with available high-value thin-film resistors (1Kohm/sq), very compact and highly functional die can be realized.

TABLE I
TYPICAL PROCESS SPECIFICATIONS

Process Specifications, $V_{ds} = 3.0 \text{ V}$		
Parameter	Typical Value	Units
E/D Lg	0.35 / 0.25	μm
D-Vp	-0.85	V
E-Vp	0.3	V
E/D-Ron	1.0 / 0.7	$\Omega \cdot \text{mm}$
D-C-off	200	fF/mm
E/D BV	12 / 12	V
D-Imax/Idss	600 / 325	mA/mm
E-Imax	400	mA/mm
D-Gm	525 @ 50% Idss	mS/mm
E-Gm	950 @ 50% Imax	mS/mm
D Ft / Fmax	55 / 125 @ Idss	GHz
E Ft / Fmax	45 / 115 @ 50% Imax	GHz
Process Elements		
Parameter	Typical Value	Units
Resistors	50 / 125 / 1000	Ω/sq
BLMET (1.0um)	30	$\text{m}\Omega/\text{sq}$
Met 2 (4um)	6	$\text{m}\Omega/\text{sq}$
MIM Cap	0.62	fF/ μm^2

III. SP7T DESIGN

The SP7T switch demonstrated in this paper, is shown schematically in Fig. 3, includes series and shunt arms, a 3:8 decoder and high Q blocking capacitors on all paths. A single control line from the decoder circuit to the common gate resistors (Rgg1..Rgg7) are used to control each throw connecting directly to the antenna port. The output inductances are external to the GaAs die using 1 mil gold bondwires and are used to match the switch for optimal insertion loss.

Due to the narrow ohmic-to-ohmic spacings, the die size was contained to only 1.6 mm x 1.2 mm. As compared to other 0.5um pHEMT processes, these FET cells are about

25% smaller. With the exception of common gate resistors, Rgg, all paths are identical in numbers of series and shunt FETS, drain to source resistors and capacitors values. This switch circuit topology is used to generate the data reported in the subsequent measurement section.

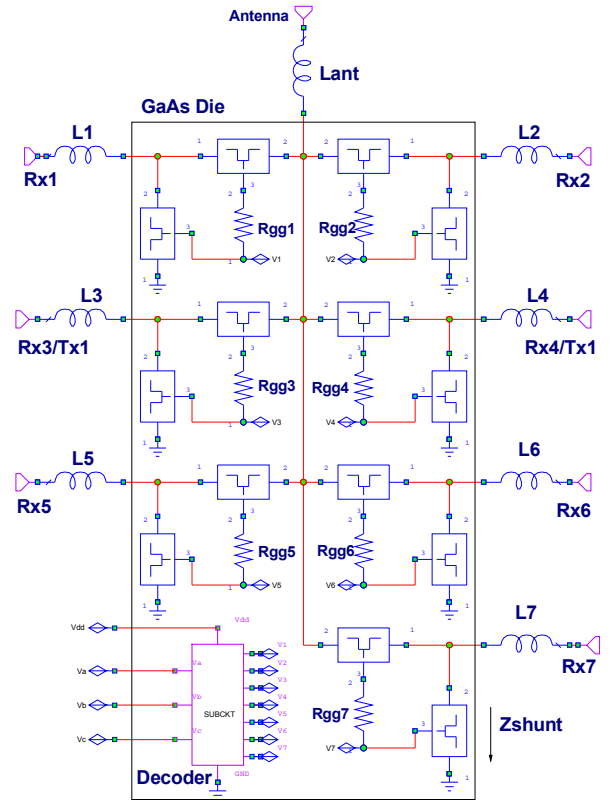


Fig. 3 SP7T switch uses series-shunt topology on all throws, 7 different gate resistors, a 3:8 decoder, and off-die bondwires for optimal matching.

IV. MEASUREMENTS

A. Isolation

Isolating the transmit (Tx) paths from receive (Rx) paths is paramount in cellular switch applications, in that poor isolation can lead to Rx de-sense, degraded harmonics or degraded linearity. In a positive controlled switch using shunt capacitors, the isolation is set by equivalent off capacitance of the FETs in series and the shunt impedance to ground of the isolated port. With Tx1 path transmitting, the isolation between Tx1 and Rx6 was measured and is shown in Fig. 4. These adjacent paths gave the worst case isolation of 33dB through 2GHz, which is well within the typical front end switch requirements.

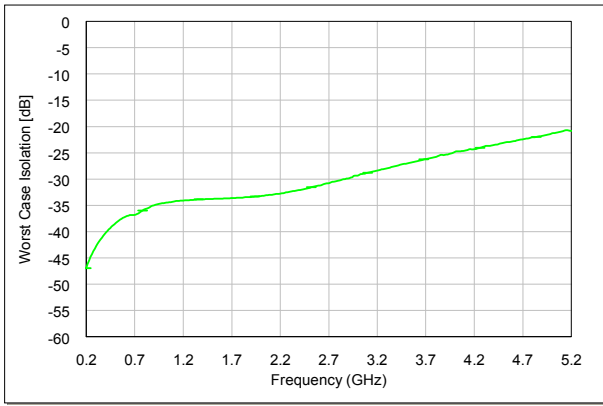


Fig. 4 Measured isolation. Worst case isolation, path Tx1 to Rx6 with Tx1 "on".

B. Insertion loss

As the design requirements of handsets becomes ever challenging, it is important for module integrators to get the most out of the switch design. Due to the needs for longer battery life, for example, maximizing PAE demands a thorough understanding as to where any losses originate.

In order to fully characterize losses, the switch designer must be cognizant of the various effects of both the equipment and the matching environment. Extreme low loss switch elements, such as a MEMs device, can have very low insertion losses [7], which can push the limits on standard VNA equipment. The SP7T switch in this paper was measured on an Agilent 5070B and the accuracy of our VNA was quantified to about 0.04dB, or about a 10% error in insertion loss [8].

More important than measurement accuracy for low loss switches, is an awareness and understanding of the mismatch losses. Fig. 6 shows how the insertion loss can be improved with improved return loss. This was demonstrated in measurements with the following graphs. In Fig. 7 we have a marginally matched Rx path with a return loss (S11 [dB]) of -15dB. The insertion loss is very good (<0.5dB), but through careful matching techniques we decrease the losses by more than 0.1dB. Fig. 8 shows the performance improvement in the same SP7T switch by adjusting the bondwire lengths. The return loss improves to -30dB and the low band insertion loss is 0.34dB over a narrower band. Likewise, a highband path was also matched to give 29dB return loss and 0.38dB insertion loss.

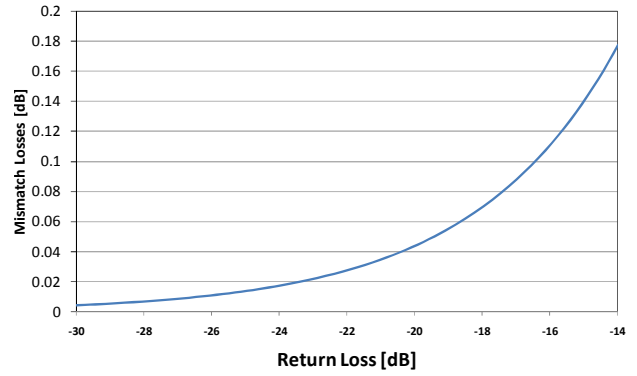


Fig. 6 Mismatch losses vs. return loss.

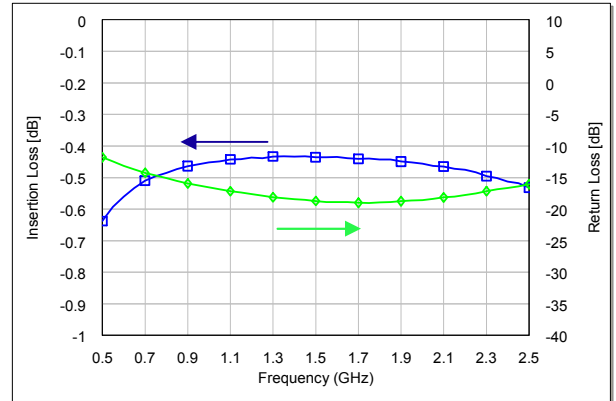


Fig. 7 Low-Band measured Insertion loss and Return loss from a marginally matched SP7T switch.

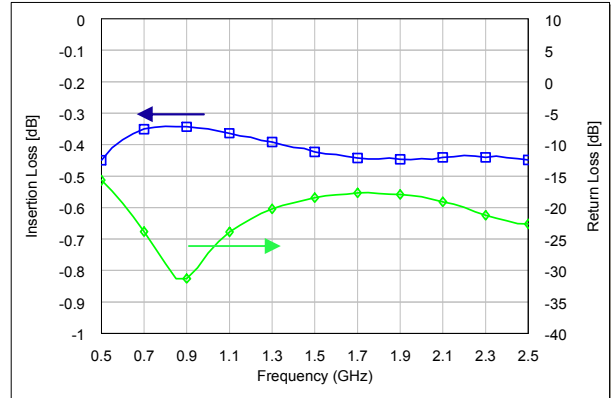


Fig. 8 Low-Band measured Insertion loss and Return loss after optimizing the I/O match in the same SP7T switch.

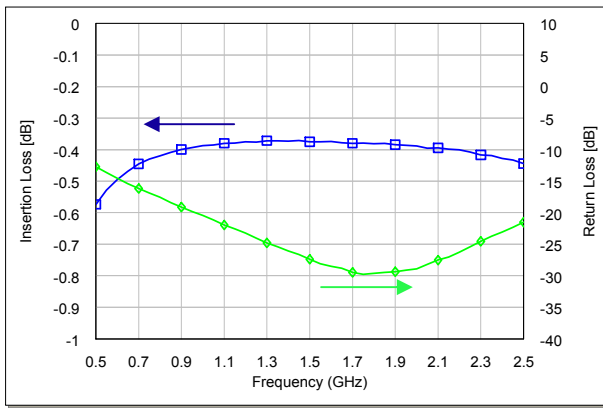


Fig. 9 Matched SP7T matched for high band insertion loss.

C. Large-Signal Measurements-Harmonics

No cellular switch design is complete without good harmonic performance. Intimate knowledge of the process is critical to the success of a product. Sizing the gate resistors to maintain high enough gate-source voltage on the off-devices is not trivial.

With the fundamental input power at 34dBm and rotated about a 3:1 VSWR load circle, the harmonics were measured on all paths. The Tx paths use 10kOhm to 12kOhm lower common gate resistors than the Rx paths and thus can handle more power. From the table below the harmonics reach an acceptable level (-36dBm or 70dBc) for both the Tx paths. Even though the Rx paths require a much lower power level (24dBm) they are near compliant to the higher GSM requirements.

TABLE II
MEASURED HARMONICS

Fo=915MHz	Pin =34dBm	Maximum Harmonic Levels Load VSWR = 3:1	
		H2 [dBm]	H3 [dBm]
Rx1	Rg0	-35.8	-27.9
Rx2	Rg0- 2K	-36.2	-29.5
Rx3	Rg0 - 4K	-36.8	-30.2
Rx4	Rg0 - 6K	-37.1	-30.6
Rx5	Rg0 - 8K	-37.5	-34.2
Rx6/Tx2	Rg0 - 10K	-38	-36.3
Rx7/Tx1	Rg0 - 12K	-39	-36.5

D. Linearity – IMD2/IMD3

Switch linearity is a sensitive topic for semiconductor foundries and is a challenging spec to meet. Reference [9] states that -105dBm is the minimum number specified to guarantee that the baseband receiver does not become desensitized. Band I IMD2, in which the interferer frequency at the antenna comes in at 190MHz, is often the most challenging of the linearity specifications. Fortunately, the switch integrator has a window in which to control the phase of the interferer signal to meet such low power levels. IMD3 was measured with an interferer at 1760 MHz and was better

than Band I IMD2 for most of the phase window, as shown in Fig. 10.

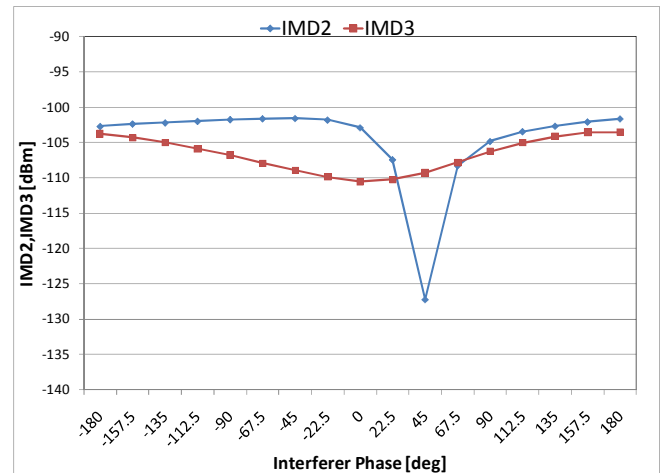


Fig 10 Linearity was measurements for Band I (1900 MHz).

V. CONCLUSION

A state of the art pHEMT process has been demonstrated to meet the latest demands of cell phone SP7T architectures. With the low Ron*Coff figure of merit and a low insertion loss of 0.5dB across the bands, a very competitive SP7T switch was reported. A compact die size was achieved due to the aggressive cell sizing employed on this switch process.

VI. ACKNOWLEDGEMENT

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VII. REFERENCES

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