G7 (QED/A 2) Process Monitor Report for FAB 3 Q2 1998

Abstract

The purpose of this work was to establish a standardized program for ongoing monitoring of process reliability. Reliability testing was previously done in order to qualify processes in the new Fab 3 facility in Hillsboro, Oregon. This qualification data provided an initial baseline on which to build the monitor program, and much of the monitor duplicates these previous tests. In addition, biased lifetests of capacitors and interconnect were added. Wafer level experiments were performed on individual devices (FETs) to determine lifetimes, and additional experiments were performed on packaged parts in an attempt to verify the wafer level results. G7 (QEDA2) was selected as the initial process to undergo the monitor testing.

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Purpose

The purpose of this work was to establish a standardized program for ongoing monitoring of process reliability. Reliability testing was previously done in order to qualify processes in the new fab facility at Dawson Creek. This qualification data provided an initial baseline on which to build the monitor program, and much of the monitor duplicates these previous tests. In addition, biased lifetests of capacitors and interconnect were added. Wafer level experiments were performed on individual devices (FETs) to determine lifetimes, and additional experiments were performed on packaged parts in an attempt to verify the wafer level results. G7 (QEDA2) was selected as the initial process to undergo the monitor testing.

Run History

QEDA2 Run 15619 was received in January, 1998. The run was fabricated using B4193A, a mask set specifically designed for reliability testing. There were 12 wafers in the run. With the exception of MIM PSN, all wafers received Mattson PSN at all layers, which was standard at the time of processing. All wafers passed post cap dc test. Two wafers were sawn in order to package parts for biased lifetesting. Two other wafers were selected for autoclave and 275ºC air bake. Two wafers were used for wafer level test experiments.

Monitor Testing

Air Bake of wafer 88543 was performed for acceleration of thermally activated failure mechanisms. A temperature of 275ºC was chosen for maximum acceleration without compromising the dielectric material. Test points were at 0 and 168 hours.

Autoclave of wafer 88544 followed JEDEC Standard Number 22, Method A102-B. The purpose of this test was to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture to the wafer. The test condition consisted of 121ºC with a 100% relative humidity at two atmospheres. Test points were at 0 and 96 hours.

Wafers 88545 and 88546 were sawn and individual die packaged from each wafer. The parts were packaged in house in open cavity ceramic 24 pin DIPs. Capacitors of 25Kum2, 50Kum2, 100Kum2, 200Kum2, 400Kum2 and 800Kum2 were biased at 15V at a temperature of 125ºC for 1500 hours with test points at 0, 168, 336, 504, 1008 and 1512 hours. Interconnect consisted of long paired meanders of 2.0um wide/4.0um pitch Metal0, Metal1, Metal2 and Metal3 lines. These were operated at a constant voltage with added resistance calculated to produce the maximum rated current densities at room temperature. For metals 1, 2 and 3, the added resistance was approximately five times the line resistance; for metal0, the added resistance was approximately three times the line resistance. The parts were operated for 1500 hours with test points at 0, 168, 336, 504, 1008 and 1512 hours. The currents used were the following: 18mA for metal 3, 7mA for metals 1 and 2, and 3mA for metal0. E and D-FETs were also packaged and used for correlation with wafer level experiments. Gate lengths were 0.6um with widths of 50um. Each FET was surrounded by a U-shaped NiCr resistor to be used for on wafer heating for acceleration of thermally activated failure mechanisms.

Wafers 88551 and 88552 were used for wafer level experiments on FETs. The same E and D-FETs described above were used for wafer level experiments. Gate lengths were 0.6um with widths of 50um. Each FET was surrounded by a U-shaped NiCr resistor to be used for on wafer heating for acceleration of thermally activated failure mechanisms.

Results

Wafer Bake

Wafer bake results are given in table 1. This table shows only structures that had less than 90% starting yield or structures that had significant degradation during autoclave. Please note that many more structures which had no anomalies and no changes are not shown. This table summary shows only the change results and does not attempt to summarize the stability of the majority of structures stressed during the wafer bake. Illegal design rule structures are highlighted. The shaded structures are in violation of layout design rules and are included for information purposes only.

Table 1 Summary. Wafer 88543, 168 hours in Air Bake at 175ºC .

Structure	Parameter Measured	Yield	% Yield	Mean	Yield after stress	Mean after stress	% change in mean
M1M2 high density, 25K 1x1 vias	Resistance	**15**	71.43	0.1315	15	0.1279	-2.74%
M1M2 high density, 25K 1x1vias	Resistance	**15**	71.43	0.1318	15	0.1282	-2.73%
M0M3 high density, 25K 1x1 vias	Resistance	**7**	33.33	0.3544	7	0.3495	-1.38%
M0M3 high density, 25K 1x1vias	Resistance	**10**	47.62	0.3555	10	0.3508	-1.32%
Ohmic-to-M1, 1x4 via1 chain	Resistance	20	95.24	0.3984	**19**	0.4112	3.21%
M0M1 30x150 via chain	Resistance	21	100.00	0.4286	**20**	0.4312	0.61%
M0M3 low density, 30x300 chain	Resistance	**16**	76.19	0.7912	16	0.8365	5.73%
M0M3 30x300 with wide pad	Resistance	**15**	71.43	0.8284	**14**	0.9292	12.17%
M0M3 10x300 via chain	Resistance	**17**	80.95	1.258	17	1.31	4.13%
Ohmic-to-M0 contact chain	Resistance	**18**	85.71	0.4611	18	0.4438	-3.75%
Capacitor, 25Kum2	Leakage at 15V	21	100.00	4.69E-09	21	1.03E-08	119.62%
Capacitor, 50Kum2	Leakage at 15V	21	100.00	9.41E-09	21	2.01E-08	113.60%
Capacitor, 100Kum2	Leakage at 15V	21	100.00	1.76E-08	21	3.77E-08	114.20%
Capacitor, 200Kum2	Leakage at 15V	20	95.24	3.63E-08	20	7.77E-08	114.05%
Capacitor, 400Kum2	Leakage at 15V	21	100.00	6.80E-08	21	1.39E-07	104.41%
Capacitor, 800Kum2	Leakage at 15V	20	95.24	1.39E-07	20	2.93E-07	110.79%

All results are consistent with expectations. The significant increase in capacitor leakages following bake (on the order of 100%) nevertheless resulted in capacitors with lower total leakages after 168 hours at 275ºC than recorded in previous tests on similar capacitors. No capacitors were lost during the wafer bake.

Wafer Autoclave

Wafer autoclave results are given in Table 2. This table shows only structures that had less than 90% starting yield or structures that had significant changes during autoclave. This table summary shows only the change results and does not attempt to summarize the stability of the majority of structures stressed during the wafer bake. Please note that many more structures which had no anomalies and no changes are omitted. Illegal design rule structures are highlighted. The shaded structures are in violation of layout design rules and are included for information purposes only.

Table 2 Summary. Wafer 88544, 96 hour Autoclave Results.

Structure	Parameter Measured	Yield	% Yield	Mean	Yield after stress	Mean after stress	% change in mean
M0M1 high density, 25K 1x1 VC	Resistance	**18**	86%	0.1772	18	0.1755	-0.96%
M2M3 high density, 25K 1x1 VC	Resistance	**18**	86%	0.113	18	0.1123	-0.62%
M2M3 low density, 30x300 VC	Resistance	21	100%	0.4234	**18**	0.4338	2.46%
M2M3 low density, 30x300 VC	Resistance	21	100%	0.4211	**20**	0.4321	2.61%
M0M3 low density, 30x300 VC	Resistance	**15**	71%	0.8056	15	0.9789	**21.51%**
M0M3 low density, 30x300 VC	Resistance	**16**	76%	0.7886	16	0.8141	3.23%
M0M3 30x300 with wide pad VC	Resistance	**17**	81%	0.7956	17	0.9437	18.61%
M0M3 30x150 Via Chain (VC)	Resistance	**16**	76%	0.514	16	0.5229	1.73%
M0M3 10x300 span Via Chain	Resistance	**16**	76%	1.27	**14**	1.287	1.34%
M0M3 5x300 span Via Chain	Resistance	19	90%	3.31	**18**	3.272	-1.15%
M2M3 high density, 16K 1x4 vias	Resistance	21	100%	0.08692	**20**	0.0843	-3.01%
Gate-to-M0 contact chain	Resistance	**18**	86%	0.315	**15**	0.3103	-1.49%
Ohmic-to-M0 contact chain	Resistance	21	100%	0.4759	**20**	0.4945	3.91%
NiCr-to-M0 contact chain	Resistance	20	95%	21.61	**19**	21.99	1.76%
Capacitor, 100Kum2	Leakage at 15V	21	100%	1.66E-08	**20**	1.56E-08	-6.02%
Capacitor, 400Kum2	Leakage at 15V	21	100%	6.94E-08	**20**	6.45E-08	-7.06%
Ohmic TLM, 2.0um wide	Sheet resistance	21	100%	125.4	**20**	125.8	0.32%
Ohmic TLM, 2.0um wide	Contact resistance	21	100%	197.2	**20**	189.5	-3.90%
EFET, 0.6x50um gate	Threshold voltage	21	100%	0.024	21	0.0554	**130.83%**
EFET, 0.6x50um gate	Id at Vd=1.5V, Vg=.7	21	100%	8.96E-05	**10**	*	*
EFET, 0.6x50um gate	Ig at 3.0V	21	100%	9.42E-10	21	1.20E-09	**27.39%**
EFET, 0.6x50um gate	Breakdown	21	100%	13.8	21	14.5	5.07%

* 11/21 EFETs failed for low current following autoclave. Decreases in Id ranged from a low of 8% to a high of 73% (site 1). Site 1 also had a Vth of 244mV. The median decrease in Id for all sites was 21.2%.

Most results are consistent with expectations. Two of the 126 capacitors were found to be shorted after 96 hours in autoclave. The sizes of the two shorted capacitors were one each 100Kum2 and 400Kum2. Three of 38 gate-to-metal0 contact chains had anomalously high resistances following stressing, as did one of 83 NiCr resistors, and one of 21 ohmic TLM structures. Finally, eleven of 21 EFETs had low drain current following autoclave. Decreases in drain current ranged from a low of 7% to a high of 73% (site 1). Site 1 also had an increase in threshold voltage to 244mV. The median decrease in drain current for all EFETs was 21.2%. The threshold voltage, gate current (Ig), and breakdown are shown for EFETs for information purposes since several FETs had channel current shifts.

Capacitor Biased Lifetest

Results of biased lifetest of capacitors is given in table 3. All of the smaller capacitors were robust through 1500 hours at 15V bias. Note that one 400Kum2 capacitor was shorted at initial test. Two additional 400Kum2 capacitors were shorted following 168 and 1008 hours respectively. A total of three 800Kum2 capacitors shorted during the 1500 hour test, one at 336 hours and two at 1500 hours.

Table 3. Capacitor Yield v. Area during 15V Biased Lifetest at 125ºC.

Capacitor Area	Initial	168 hours	336 hours	504 hours	1008 hours	1512 hours
25Kum2	24/24	24/24	24/24	24/24	24/24	24/24
50Kum2	24/24	24/24	24/24	24/24	24/24	24/24
100Kum2	24/24	24/24	24/24	24/24	24/24	24/24
200Kum2	24/24	24/24	24/24	24/24	24/24	24/24
400Kum2	**23/24**	**22/23**	22/22	22/22	**21/22**	21/21
800Kum2	24/24	24/24	**23/24**	23/23	23/23	**21/23**

Interconnect Biased Lifetest

Results of biased lifetest of interconnect is given in table 4. All of the metal lines showed a net decrease in resistance over the 1500 hour period of the test. There were no failures. Oven temperature was 125ºC, and hot spot temperature was estimated based on thermal analysis to be approximately 160ºC.

Table 4. Interconnect biased lifetest at maximum rated current density, 1500 hours.

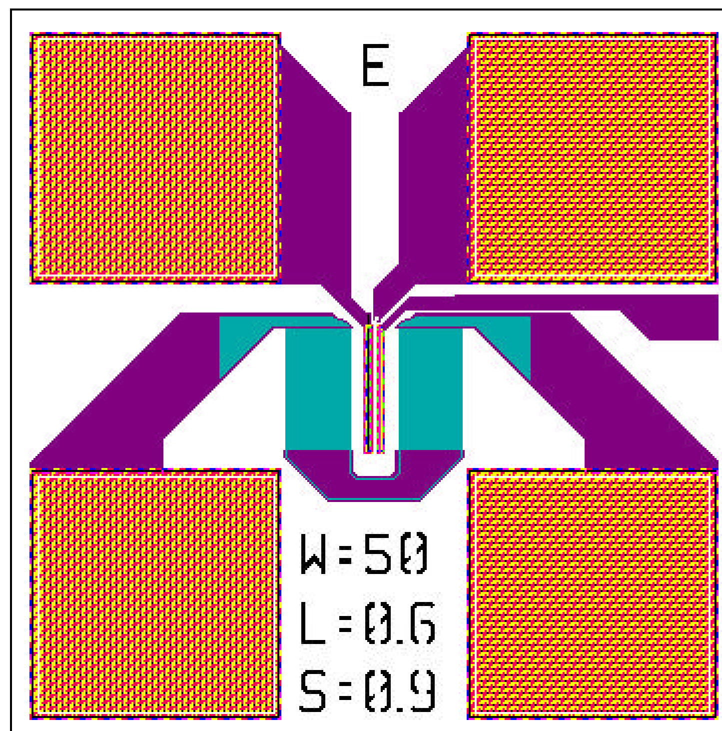
Interconnect Layer	Number of Parts	Average Percent Change in Resistance
Metal3	48	-1.1
Metal2	24	-1.4
Metal1	48	-1.2
Metal0	48	-0.9

Wafer Level Testing: FET Lifetimes

Field effect transistors with a gate length of 0.6um and a gate width of 50um (0.6x50um FET) were selected. Figure 1. shows an enhancement mode FET (EFET, normally off) with Metal0 (purple or dark solid regions) connections to the bond pads. The source connection extends to an additional pad on the right hand side (not shown.)

A NiCr resistor (teal or light solid regions in Figure 1.) surrounds the width of the EFET. The NiCr resistor serves as a heater, and is a 25x50um rectangle located 6um away on both sides of the EFET and connected to the bond pads using metal0. The resistance of the NiCr heater at room temperature is just over 200Ω.

Figure 1. Metal0 Connected EFET with NiCr Heater



Heater Characterization:

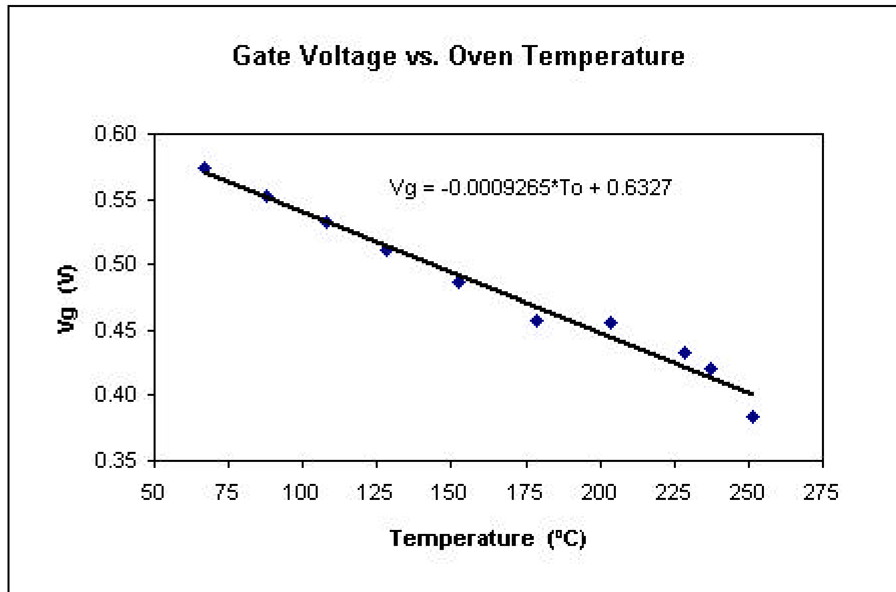
A packaged EFET was used for heater characterization. With the drain and source grounded on the EFET and the gate connected to a constant current supply and an ohmmeter, the EFET was operated as a temperature sensing diode. The system was heated in an air bake oven. The temperature of the oven was determined using a J-type thermocouple set directly above the packaged EFET.

Temperature was stepped from approximately 20ºC to 250ºC. Resistance measurements were taken at each step only after the temperature in the oven chamber had reached equilibrium. One-half milliamp was forced through the EFET, and the resistance of the gate was measured. The gate voltage was calculated from the measure resistance. These data points were collected and plotted. A line was fitted (Figure 2.) to the raw data points from which a gate voltage versus oven temperature slope was extracted. The clalculated equation of the line was found to be:

$$V_g = -0.0009265 \cdot T_o + 0.6327 \quad \textbf{(1)}$$

where T_o is the temperature of the air bake oven and V_g is the calculated gate voltage.

Figure 2.



Next, an *on wafer* EFET of the same parameters as above was set up on a Rucker and Kolls 680 wafer prober. Parametric tests were done with a Keithly Instruments, Inc.® Yieldstation™ S900. Test codes were written using S900A Autogen Version 4.1 which utilizes Microsoft® Visual Basic for MS-DOS™.

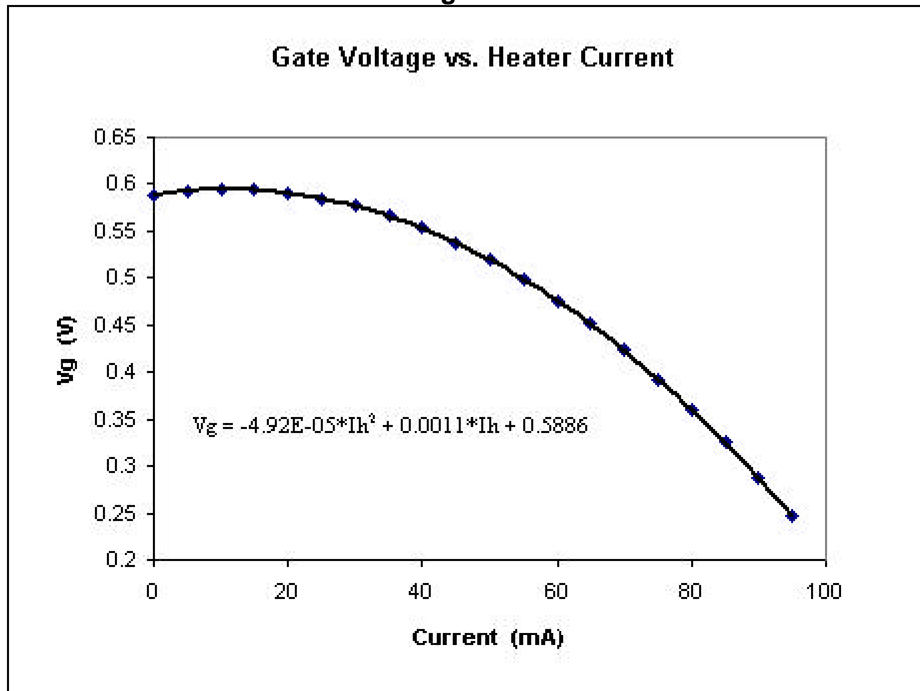
The same electrical test was repeated with the on wafer EFET, with the resulting response being a resistance reading. During this test, a current was forced through the NiCr heater surrounding the EFET to produce the heat source instead of an air bake oven.

Current through the heater was stepped from 0mA to 60mA in increments of 10 mA, and the resulting resistance was observed. The gate voltage was calculated and plotted, to which the following equation was fitted:

$$V_g = -4.92E-05 \cdot I_h^2 + .0011 \cdot I_h + 0.5886 \qquad \textbf{(2)}$$

where I_h is the current forced through the NiCr heater and V_g is the gate voltage calculated from the measured resistance. Figure 3. shows the curve of the results obtained during this experiment.

Figure 3.



The heater can now be characterized by setting equations (1) and (2) equal to each other. The variable T_o becomes T_a which represents the ambient temperature sensed of the EFET by use of the NiCr heater only.

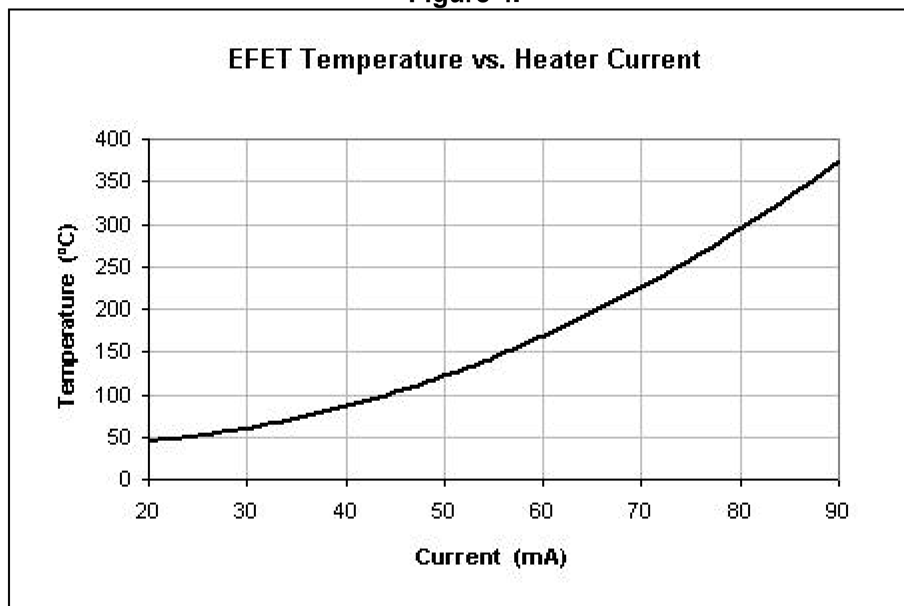
$$-0.0009265 \cdot T_a + 0.6327 = -4.92E-05 \cdot I_h^2 + 0.0011 \cdot I_h + 0.5886 \qquad \textbf{(3)}$$

Solving for T_a, equation (3) becomes:

$$T_a = -0.0531 \cdot I_h^2 - 1.164 \cdot I_h + 47.61 \qquad \textbf{(4)}$$

where I_h is controlled in this experiment by forcing a current though the NiCr heater, and T_a is the resulting temperature of the EFET due to the power dissapation of the heater.

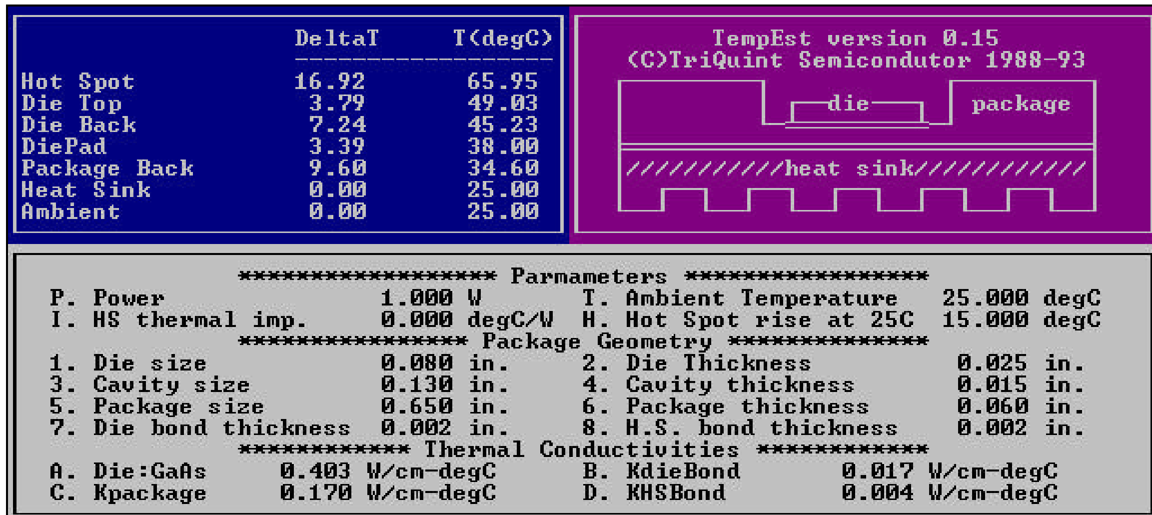
Figure 4.



EFET Heat Dissipation Calculation:

To determine the self-heating of the EFET (if any) when turned on hard, a program called TempEst, created by TriQuint employee Dave Smith, was used. It is based on a model which includes thermal conductivities of the materials being used and some simple approximations for the geometries. TempEst is believed to produce reasonable estimates of peak temperatures with the utilization of limited input information. An example screen is shown in Figure 5.

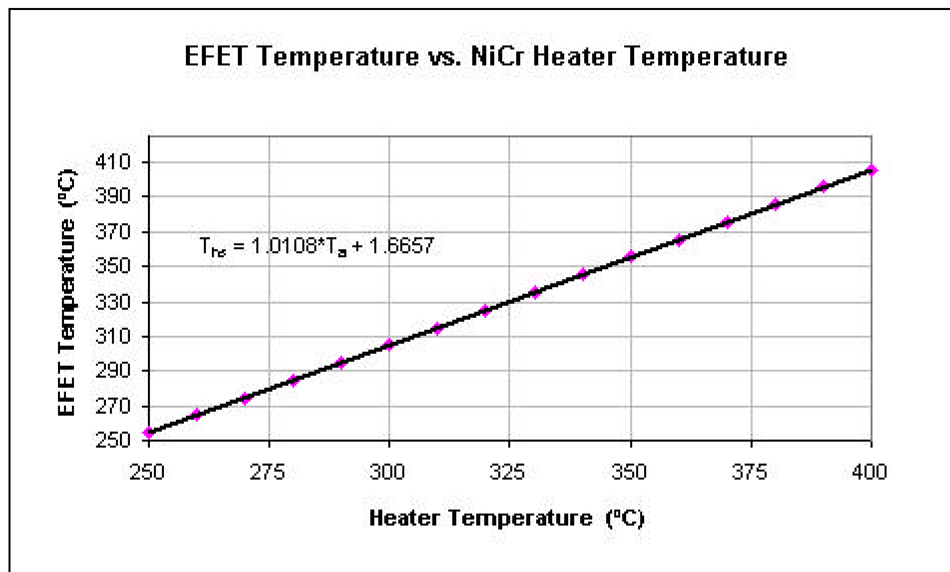
Figure 5.



This program assumes that the element is in a packaged part. Package Geometry values are negligible because the heater is the main source of the heat which is in close proximity to the EFET. "...typical individual devices will occupy only a small portion of the top surface of the device. Now let us imagine that this device is not part of an integrated circuit, but just a small entity mounted all alone on a relatively large GaAs chip. To this very small device, the die attach, chip edges, package and heat sink look very far away indeed. In fact for this small device, we might as well consider the heat sink to be at infinity. Calculations using this approach will yield increasingly accurate results as the device size becomes smaller with respect to the chip size (Smith, David H. and Fraser, Arthur*, Measurement and Prediction of Operating Temperatures for GaAs ICs*, p. 3, 1986)."

Heater or ambient temperatures, T_a, of 250ºC to 400ºC (refer to Figure 4 for corresponding heater current values) were entered into the program and the resulting hot spot temperatures of the EFET, T_{hs}, values were as follows:

Figure 6.



T_{hs} values ranged from 4.3ºC to 6.0ºC for the above range of heater temperature values.

Thermal infrared analysis was also used to estimate the heat dissipation of the EFET. Based on this technique, the operating EFET was estimated to produce self heating of approximately 3C. The overall temperature of the heater and the EFET when turned on hard is only slightly higher than the ambient temperature created by the NiCr heater alone. Therefore, the heating effect of the EFET contributes very little to the overall ambient temperature.

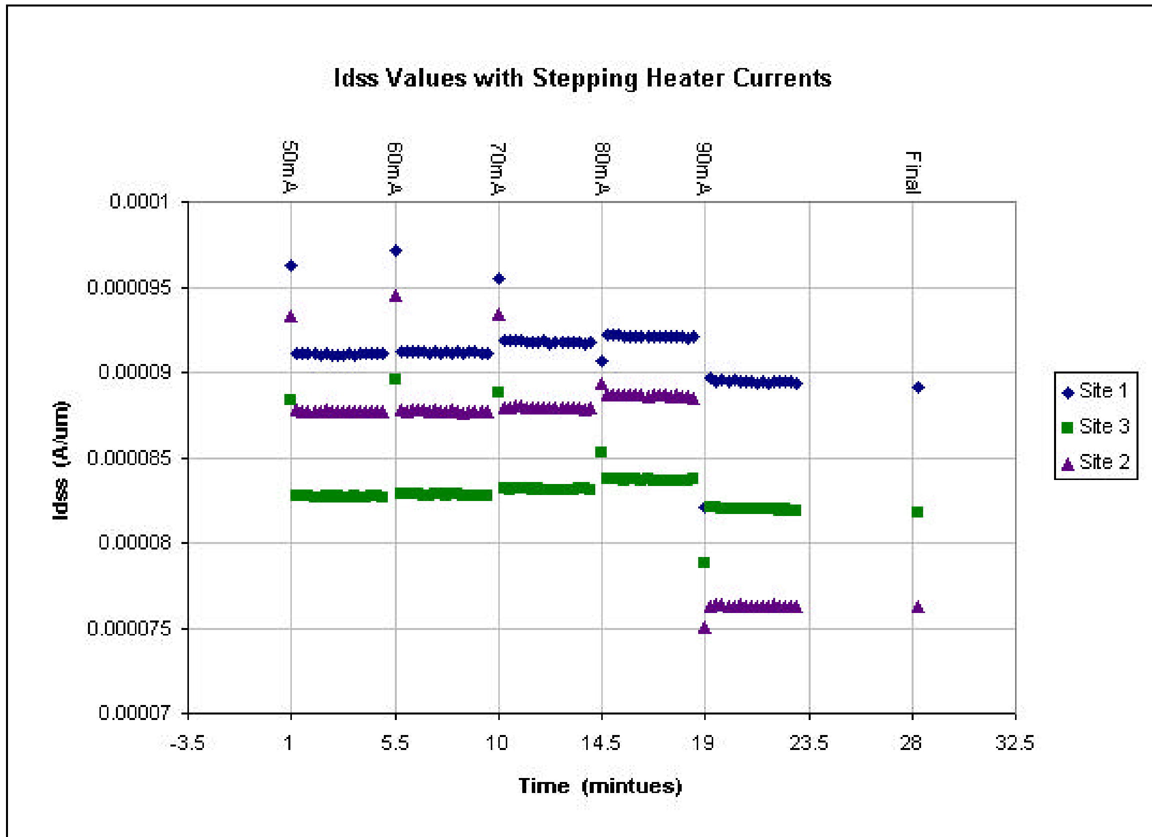
FET Lifetimes:

With the FET turned on hard, a shift of twenty percent in drain current (Id) from the initial Id value was selected as the failure criterion limit. Using the estimate of the ambient temperature created by the forced heater current, the following experiment was performed to establish appropriate starting points at which to stress FETs to failure.

The heater current was turned on for thirty seconds beginning at 0mA. At the end of the thirty second interval, an Id measurement was taken and the heater immediately turned off. Id measurements were then taken at ten second intervals for four minutes before stepping the heater up to the next 10mA interval. This experiment was continued to 90mA heater current. Current values over ~90mA producing estimated temperatures of over 375ºC could not be used since they were found to cause damage (discoloration) to the overlying polymer dielectric (BCB).

No changes in Id were observed for current values of 0mA up to 70mA. After heating for thirty seconds, Id returned to values comparable to the initial Id value. Slight shifts were observed after heating for thirty seconds at 80mA and 90mA. Figure 7. gives values obtained on three different sites for heater currents of 50 to 90mA.

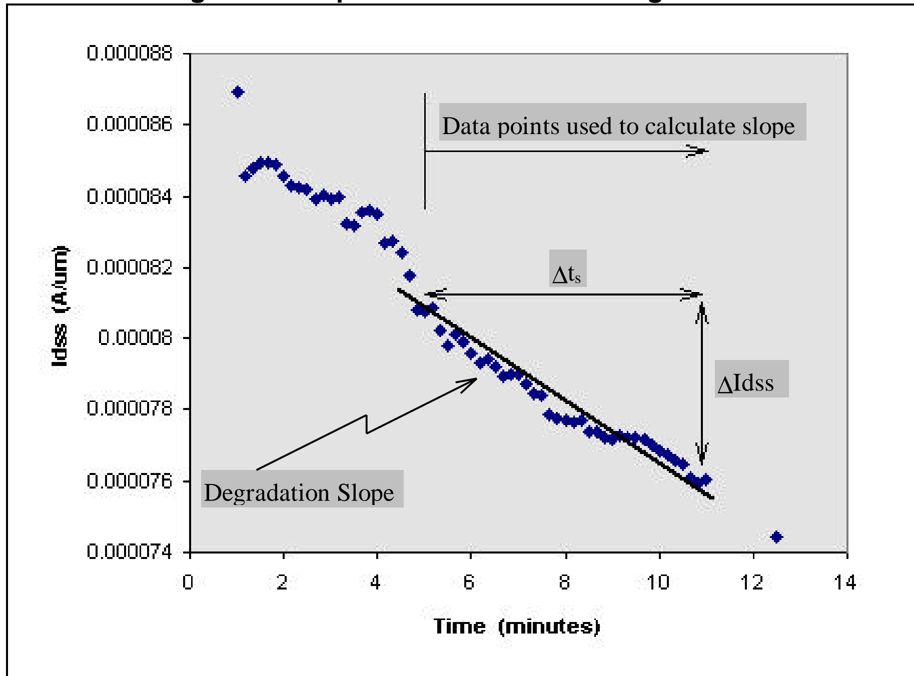
Figure 7.



Based on the previous experiment, currents between 80mA and 90mA were chosen to stress FETs to failure. All EFETs were turned on hard with 2.5V on the drain, 0.7V on the gate and the source grounded. An initial Id measurement was taken after turning on the FET for sixty seconds. Once the heater was turned on, Id measurements were taken continuously at ten second intervals. At the conclusion of stressing the FET, a final Id measurement was taken with the heater off for comparison with the initial Id measurement.

The data was plotted (Id v. time) as in Figure 8, and the following procedure was used to estimate time to failure. The first point in Figure 8 is the initial Id value. There was typically a drop in Id that occurred immediately after the heater was turned on. During the first few minutes of stressing, a “stabilization” seemed to occur on Id measurements. Following this period, the Id measurements began a more steady decline. This region was selected in order to calculate the slope of the degradation. The calculation of the slope ends at the point where the Id values begin to plateau.

Figure 8. Slope Estimation of FET Degradation



In Figure 8. for example, a 10.2% shift in Id occurred over 6.5 minutes. Since our failure criterion is a shift of twenty percent, the time needed for a shift of twenty percent to occur was estimated to be 12.7 minutes (6.5 minutes x 20/10.2).

Table 5. gives the results obtained on 25 different EFETs operated at four different temperatures (heater currents) along with their estimated times to failure.

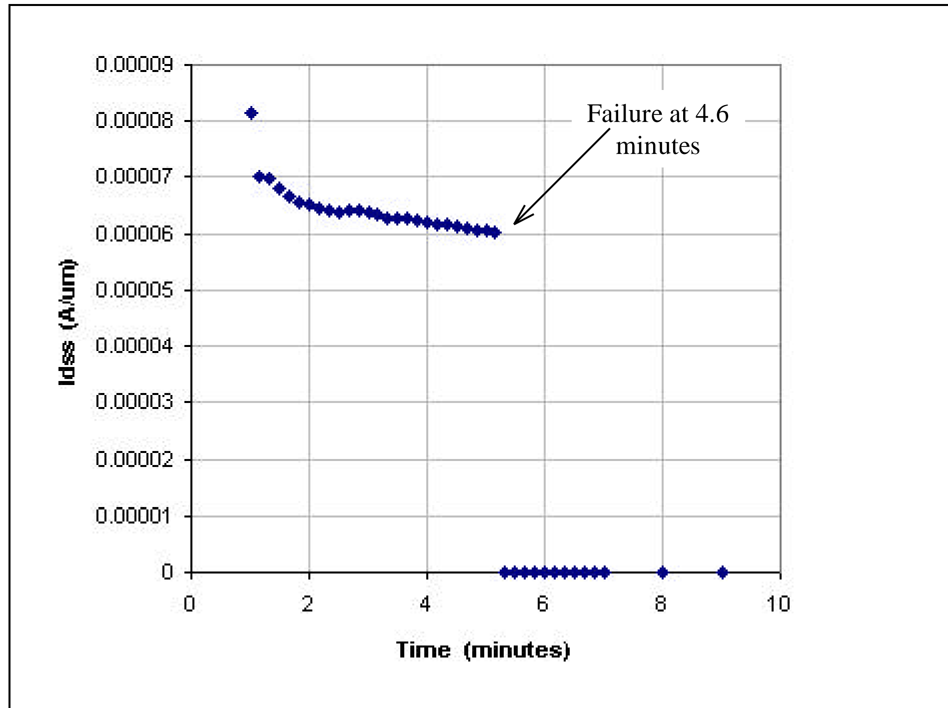
Table 5.

Wafer (#)	Site (#)	Current (mA)	Idss Change (%)	Time (minutes)	Estimated Time to 20% (minutes)	Degradation Slope ($\Delta Idss/\Delta t_s$)
88552	2,0	89	12.4	3.1	5	-0.6876
88552	2,1	89	11.8	3.7	6.3	-1.069
88552	2,2	89	14.8	4.2	5.7	-1.552
88552	2,3	89	12.7	3.8	6	-1.0498
88552	2,4	89	19.2	4	4.2	-1.7506
88552	2,5	89	14.3	1	1.4	-1.5561
88551	2,3	87	21.69	10	9.22	-1.3995
88551	2,4	87	25.03	10	8	-0.6212
88551	3,2	87	2.53	1.6	12.6	-1.7869
88551	4,1	87	9.1	12	26.4	-0.6676
88551	4,3	87	1.7	4	47	-0.4942
88551	5,4	87	1.6	1	12.5	-1.6253
88551	6,1	87	3.7	12	65	-0.4046
88552	1,0	87	7.4	8.3	22.5	-0.2507
88552	1,1	87	10.2	11	21.6	-0.3112
88551	1,1	85	12.73	10	17	-1.4161
88551	2,1	85	15.54	10	14	-1.3971
88551	2,4	85	10.2	10	13	-0.9987
88551	3,2	85	10.21	6.5	13	-0.9686
88551	4,2	85	5.1	23	90	-0.2128
88551	4,3	85	9.13	5	11	-1.6559
88551	5,4	85	4.73	3.8	16	-0.9596

88551	6,1	85	5.6	7.8	27	-0.6308
88552	5,2	81	1.9	180	1918	-0.0055
88552	-1,2	81	7.1	700	1986	-0.0047

EFETs tested at heater currents of 89mA typically experienced catastrophic failures. At temperatures of approximate 365ºC, the times to failure times were on the order of 4 to 6 minutes. The failure mode was determined to be shorting between the heater and the drain, and is likely due to the very high field (>15V) between the closely spaced metal 0 lines forming the connections of the heater and and the drain to the pads. Figure 9. is an example of the typical degradation of FETs at 89mA or 365ºC.

Figure 9.



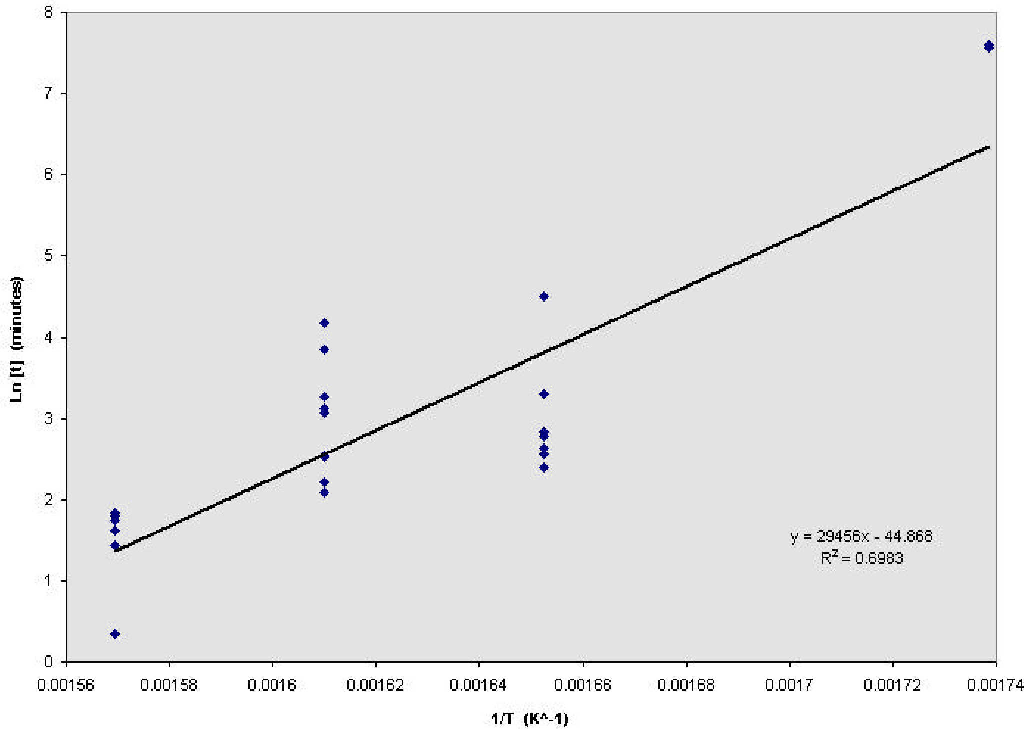
The results from Table 5 are plotted in Figure 10. An Arrhenius equation relates lifetimes and temperatures as shown:

$$t = C\exp(-Ea/kT)$$

where t = time, C is a constant, T is temperature in Kelvin, k is Boltzmann's constant, and Ea is the activation energy for the process. Taking the natural log of each side:

$$\ln(t) = -Ea/kT + \text{constant}$$

Therefore, a plot of ln(t) v. 1/T produces a line with slope Ea/k. From the slope of the line in Figure10, and using k = 8.614e-5, an activation energy of 2.54eV can be estimated for the degradation of the EFETs. This assumes a single failure mechanism, assumed based on historical data, to be sinking gates, and ignores the catastrophic failures at maximum heater current values thought to be the result of high fields.



Conclusion
A monitor program was established for ongoing monitoring of process reliability. The first quarter of the monitor program was completed using a run fabricated with the QED/A 2 process on the reliability mask set B4193A. The monitor program duplicated wafer level bakes and autoclave established in the new fab qualification procedure. Additional testing included biased lifetests of packaged capacitors and of interconnect, as well as experiments with on wafer determination of FET lifetimes.

Most of the monitor results were consistent with expectations, with the following notable exceptions:

Capacitors.

The significant increase in capacitor leakages following bake (on the order of 100%) nevertheless resulted in capactiors with lower total leakages after 168 hours at 275ºC than recorded in previous tests on similar capacitors.

A total of five large capacitors shorted during biased lifetest (15V, 125ºC, 1500 hours). The affected capacitor sizes were 400Kum^2 and 800Kum^2. The shorts occurred one each at 168 hours, 336 hours and 1008 hours, and two at 1512 hours. Smaller capacitors (25Kum^2 to 200Kum^2) were robust throughout the full 1500 hours at 15V. A total of 143 capacitors were included in the test.

Two of 126 capacitors were shorted following 96 hours autoclave. The sizes of the shorted capacitors were one each 100Kum^2 and 400Kum^2.

Due to the occurrence of the capacitor shorts noted above, continued close monitoring of capacitors is recommended. The biased lifetest will be continued indefinitely to determine median lifetimes of capacitors as a function of area.

EFETs
Low drain currents were noted on EFETs following moisture stress. Eleven of 21 EFETs had low drain current following 96 hours autoclave. The median decrease in drain current for all 21 EFETs was 21.2% following autoclave. This has been previously noted as an issue with this process, and is the subject of ongoing process improvement efforts. This is an area of concern.

Gates
Three of 38 gate to metal0 contact chains had anomalously high resistance following 96 hours autoclave. While these contact chains are not typical of functional circuits, this bears further observation, and may provide a clue to the EFET degradation noted above.

An activation energy of 2.54 eV was estimated for EFET lifetimes based on on wafer experiments. This value is consistent with historical estimates obtained on packaged parts. Additional work is needed to confirm that the more rapidly obtained wafer level results consistently conform to those obtained in more traditional packaged part/oven lifetests.

Conclusion

In summary, the first quarter of the monitor program was successful. The Q2 1998 monitor flagged two areas of concern for process improvement efforts on QED/A 2 (capacitors and EFET moisture resistance), and along with future quarterly monitors will establish a historical baseline for all processes in the Dawson Creek facility. Initial experiments indicate that rapid wafer level tests may be used to determine lifetimes and activation energies in lieu of longer package level tests, though additional work remains to verify this. The Q3 1998 monitor will be extended to cover both G7 (QED/A 2) and G16 (TQTRx).