



G7 Element Qualification Report Revision 2, 1-22-1998

Purpose

This report summarizes element qualification test results obtained on TriQuint's G7 (QED/A 2) process, fabricated at FAB 2 in Beaverton, Oregon and FAB 3 in Hillsboro, Oregon. A comprehensive series of testing was performed on wafer in order to verify successful transfer of the process to TriQuint's new facility in Hillsboro.

Method

It was determined to use three runs from FAB 3, the new facility, for comparison with two baseline runs from FAB 2. As of this writing, all five runs from the two locations have completed testing. These runs and wafers are given in Table 1. All tests were performed on whole wafers.

<i>Process</i>	<i>Location</i>	<i>Run</i>	<i>Air Bake Wafer</i>	<i>Autoclave Wafer</i>	<i>Temperature Cycle Wafer</i>
G7	FAB 3	14769	72219	72215	72211
G7	FAB 3	14939	74902	74906	74908
G7	FAB 3	15048	77080	77078	77082
G7	FAB 2	14626	72033	72060	72059
G7	FAB 2	14759	72166	72168	72167

Stresses

Air Bake was performed for acceleration of thermally activated failure mechanisms. A temperature of 275°C was chosen for maximum acceleration without compromising the dielectric material. Test points were at 0 hours, 96 hours and 168 hours. *Note:* This test is intended to produce a 20% reduction in channel current of FETs representing approximately 100 years of life at 150°C.

Autoclave followed JEDEC Standard Number 22, Method A102-B. The purpose of this test was to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture to the wafer. The test condition consisted of 121°C with a 100% relative humidity at two atmospheres. Test points were at 0 hours, 48 hours and 96 hours.

Temperature Cycle followed JEDEC Standard Number 22, Method A104-A, Condition "G." The purpose of this test was to determine the wafer resistance to alternating extremes of high and low temperatures in air. The test condition cycled at a low temperature of -40°C to a high temperature of +125°C with a ten minute dwell time at each extreme. Test points were at 0 cycles, 250 cycles, 500 cycles and 1000 cycles.

Table 2 summarizes the stresses performed.

Table 2. Stress Parameters				
<i>Test</i>	<i>Test Condition</i>	<i>Test Point 1</i>	<i>Test Point 2</i>	<i>Test Point 3</i>
Air Bake	275°C	0 hrs.	96 hrs.	168 hrs.
Autoclave	121°C, 100% RH	0 hrs.	48 hrs.	96 hrs.
Temperature Cycle	-40°C to +125°C	0 cycles	250 cycles	500 cycles

The following were exceptions to the stresses above:

FAB 2 Run 14626, Wafer 72033 was tested at 24 and 48 hours in addition to the test points given above.

Wafer 72060, from the same run, was tested at 24 and 72 hours in addition to the test points given above.

Wafer 72059 was initially started in temperature cycle at -65°C to +150°C. Due to a malfunction in one of our temperature cycle chambers, the wafer was moved to another chamber after 145 cycles. The remainder of the temperature cycling was done at -40°C to +125°C.

All wafers were continued to 1000 temperature cycles for information purposes only.

Test Structures

Six sets of structures were chosen to be analyzed for the qualification report. Table 3 gives a general description of the structures used.

Table 3. Test Structures	
<i>Structure</i>	<i>Structure Description</i>
Capacitors	Metal0 to MIM Metal; 25Kum ² , 50Kum ² , 100Kum ² , 200Kum ² , 400Kum ² and 800Kum ² areas.
Combs	1.0um, 1.6um, 2.0um and 3.0um gaps, 1800um length. Gate to Gate, Gate to Ohmic, Ohmic to Ohmic, Metal0 to Metal0, MIM Metal to MIM Metal, Metal1 to Metal1, Metal2 to Metal2, Metal3 to Metal3. Also 1.4um, 1.6um, 1.8um, 2.0um gaps for FAB 3 and 1.6um, 1.8um, 2.0um for FAB 2; 1325um lengths.
FETs	0.6um x 50um gate with 1.0um gate to drain/source distance. DFET and EFET.
Metals	Metal0, Metal1, Metal2, Metal3, NiCr, Ohmic, Gate and MIM Metal paired meanders; minimum width and pitch.
Ohmic Contacts	2x2, 4, 8um implanted TLM with minimum length ohmic contacts.
Vias/ contact chains	Metal0 to Metal1, Metal1 to Metal2, Metal2 to Metal3, MIM Metal to Metal1, Gate to Metal0, Gate to Metal1, NiCr to Metal0, Ohmic to Metal0 and Ohmic to Metal1; Via/contact chains with minimum dimension contacts.

Table 4 lists the electrical tests conducted on each of the structures. Approximately 3,300 parameters were tested per wafer.

Table 4. Electrical Tests					
Structure	Electrical Tests				
FETs	Yield	Threshold Voltage	Drain Current	Gate Current	Breakdown Voltage
Vias/contact chains	Yield	Resistance			
Capacitors	Yield	Leakage at 10 and 15V			
Metals	Yield	Resistance			
Combs	Yield	Leakage at 10V			
Ohmic Contacts	Yield	Resistance			

Special Processing Notes:

Run 14769 was processed at FAB 2 through implant anneal. There was a break in ohmic metal deposition between Ge and Au. Wafers were sent back for rework at Via3 visual inspection for “junk” on wafers. All wafers received an additional 1 minute KII2 dip. It was noted on the run sheet that there “may be some bond pad delamination from KII2...”

Run 14939 received a non-standard ohmic alloy. PSN deposition at interlayer dielectric layers (ILD) 1, 2, and 3 used recipe “C120.” Initial test of the wafers from this run showed low yield on all Metal2 to Metal3 via chains, and on Metal1 to Metal2 low density via chains, also referred to as “homers”.

Run 15048 received some early bakes, in particular a seven minute 300°C bake in nitrogen following gate plasma silicon nitride deposition (PSN).

On all three FAB 3 runs, MIM PSN was deposited in a new nitride deposition tool using recipe “C120.” FAB 2 runs received TriQuint’s standard MIM PSN.

Results

Capacitors

FAB 2 capacitors used TriQuint’s standard MIM PSN process producing better results both before and after stressing. Leakage values at 10V on all capacitor sizes were typically less than a few nanoamperes on FAB 2 wafers. Yields on the 25Kum² capacitors were consistently 100% on all wafers, and 95-100% on the largest (800Kum²) capacitors.

FAB 3 capacitors used a different Nitride deposition tool which resulted in increased capacitor leakage and reduced yield and reliability. Following these tests, G7 capacitors in FAB 3 have reverted to TriQuint’s original standard MIM PSN process for better yield, reliability and leakage values. Yield improvement efforts are on-going.

TriQuint’s standard MIM PSN process produces fully acceptable capacitor yields and reliability. TriQuint’s standard MIM PSN will continue to be used until a comparable results Nitride process can be found using the new tool.

Comb Structures

The general trend for FAB 3 and FAB 2 was a net decrease in leakage during air bake, autoclave and temperature cycle.

Table 5 gives the minimum reliably printable gap for a given layer combination in the two fabs. For both fabs, 1.6um was the minimum gap dimension measured, since this is well below the design rule minimums (2.0 or 3.0um, depending upon layer).

TriQuint's G7 process shows excellent yield and reliability for intralayer leakages based on the current design rule minimum gap spacings.

	<i>FAB 3</i>	<i>FAB 2</i>
<i>Layer</i>	Minimum Spacing	
Gate	1.6um	1.6um
Gate to Ohmic	1.6um	1.6um
Ohmic	1.6um	1.6um
Metal0	1.6um	1.6um
MIM Metal	1.6um	1.6um
Metal1	1.6um	1.6um
Metal2	1.6um	1.6um
Metal3	1.6um	1.6um

Metals

Metal0, Metal1, Metal2 and Metal3 meanders remained stable throughout stressing for both fabs, maintaining high yield values. Intralayer leakage values (Ohmic, Gate, NiCr, Metal0 and MIM) for minimum pitch lines, and interlayer leakage values (Ohmic, Gate, NiCr, Metal0 to MIM and MIM to Metal1) also remained unvarying during stress.

Anomalies noted at test on Metal3 meanders from Run 15048, Wafer 77082 and Run 14939, Wafer 74902 were manually probed and could not be confirmed. A tester issue after 96 hours bake on Run 14939 led to only 14 of 21 sites data being collected for most tests at this step.

TriQuint's G7 process for metals shows satisfactory yield and reliability for metal lines and for intralayer leakage values based on the current design rule.

Ohmic Contacts

Contact resistance was stable throughout autoclave and temperature cycling on all wafers. The FAB 2 air baked wafers had an initial contact resistance of ~170Ω. The FAB 3 wafers had higher initial contact resistance values of ~250Ω. Both fabs experienced little change in resistance due to baking. Shifts of 8-16% occurred in FAB 2 and shifts ranged from -3% to 4% in FAB 3.

Anomalies after 1000 temperature cycles on transmission line measurements (TLMs, used to derive ohmic contact resistance) from Run 15048, Wafer 77082 and after 168 hours bake on Run 14939, Wafer 74902 were manually probed and could not be confirmed. Tester issues occurred in Run 15048 at initial test, and after 96 hours bake on Run 14939. Full (all sites) data was collected at all other steps.

The results obtained from ohmic contact data demonstrates that TriQuint's G7 process for this element produces dependable yield and reliability values.

Via/contact chains

Overall, via/contact chains from both fabs showed very little movement in resistance.

Ohmic to Metal1 and Ohmic to Metal0 chains decreased in resistance or remained unchanged during autoclave and temperature cycle on all five runs.

Ohmic to Metal1 and Ohmic to Metal0 chains decreased in resistance during air bake on four wafers. On one baked wafer, Ohmic to Metal0 via chains showed an increase in per via

resistance on the order of about 15%. The Ohmic to Metal1 via/contact chain resistances increased by about the same amount on this wafer.

Metal2 to Metal3 Homers or low density via chains also showed increases in resistance, especially on the baked wafers. The largest of these was an increase of nearly 100% on Metal2 to Metal3 30um x 300um chains on wafer 72166 (FAB 2). Because this fab is no longer in operation, no further analysis of this wafer is planned. All other via/contact chains were largely stable.

The following anomalies were noted on FAB 3 via chains:

Anomalies occurred on Ohmic to Metal1 via chains on five wafers. No analysis is planned of these structures since they represent a violation of current layout design rules which forbid the placement of Via1 over Ohmic metal.

Only a single anomaly was confirmed on temperature cycled wafers from all three FAB 3 runs. This was a Metal2 to Metal3 (Via3) chain, which tested open after 1000 cycles on run 14939. This represents a single Via3 chain out of 294 Via3 chains on the wafer including a total of 1.76 million vias, which is within acceptable limits. Run 15048 had no anomalies in temperature cycling. There were four test anomalies on run 14769; however, the wafer was lost and we were unable to manually probe the sites in order to confirm these.

On autoclaved wafers, Run 15048 had no anomalies. Run 14939 had four of 215 Via3 chains and one of 279 Via2 chains that had large increases in resistance. One of 38 Ohmic to Metal0 contact chains also experienced a significant increase. Run 14769 had numerous anomalies on Via3. There were 58 of 291 total open Via3 sites on this wafer following the completion of 96 hours, and an additional seven sites with high resistance. However, there were no other via/contact anomalies on this wafer.

In bake, Run 15048 had six of 42 Ohmic to Metal0 contact chains, two of 290 Via3 chains, two of 234 Via1 chains and one of 285 Via2 chains which experienced large resistance increases over the course of stressing. Run 14939 had ten of 200 Via3 chains and one of 248 Via2 chains which increased in resistance. (Note the lower Via3 initial yield on this run). Run 14769 had four of 278 Via3 chains which measured open after completing bake, five of 274 Via3 chains, four of 264 Via2 chains and two of 248 Via1 chains that increased in resistance.

Failure analysis is on-going on these via structures at TriQuint. The current focus is on determining the root causes of the large Via3 fallout on run 14769 in autoclave, and of the Ohmic to Metal0 contact chain changes on run 15048 following bake.

TriQuint's interconnect process shows good reliability in temperature cycling. Two of three FAB 3 runs performed robustly in autoclave; however, a third run experienced difficulties with Via3. Most interconnect layers were solid in bake, but some concerns were raised about Via3 and Ohmic to Metal0 contact chains. All of the FAB 3 runs included in this report were produced during the early stages of bringing up a new via etch tool. As a consequence of these concerns, two additional runs of G7 material have been obtained in order to repeat both the bake and autoclave stresses on via structures from more recent material.

FETs

Most FET parameters remained stable through all three stresses. Note that the 275°C air bake is intended to produce a 20% reduction in channel current of FETs representing approximately 100 years of life at 150°C. Mean values of FET parameters during stressing are given in Tables 6-8.

Two FET anomalies were noted on one of the FAB 2 baked wafers. These occurred on the same site at a single test point, but both FETs were functional at the next test point. Therefore, the anomalies could not be confirmed.

No FET anomalies were noted on the remaining 14 wafers under test.

Although some FET parameters had large percentage changes between initial and final test, most values stayed well within guaranteed specification ranges. For example, DFETs had increases in gate current ranging up to 77%, but values fell well within the $\leq 5\text{nA}/\mu\text{m}$ guaranteed specification range. Results obtained from testing TriQuint's FETs has shown them to be high in both yield and reliability.

Table 6. Mean FET Parameters for Air Baked Wafers						
Site	Run	Test Point	V_{th} (V)	I_d (mA/ μm)	I_g (nA/ μm)	BV_{GD} (V)
DFETs						
FAB 2	14626	0 hrs.	-0.552	0.050	0.172	17.276
		96 hrs.	-0.550	0.049	0.166	17.201
		168 hrs.	-0.545	0.049	0.155	17.094
		Total Percent Change	-1.28%	-3.04%	-11.23%	-1.06%
FAB 2	14759	0 hrs.	-0.458	0.037	0.140	15.992
		96 hrs.	-0.443	0.032	0.123	15.959
		168 hrs.	-0.428	0.031	0.123	15.928
		Total Percent Change	-7.02%	-19.13%	-13.86%	-0.40%
FAB 3	14769	0 hrs.	-0.684	0.068	0.319	20.362
		96 hrs.	-0.712	0.037	1.321	16.759
		168 hrs.	-0.681	0.057	1.395	16.404
		Total Percent Change	-0.44%	-19.38%	77.10%	-24.13%
FAB 3	14939	0 hrs.	-0.327	0.021	0.098	19.742
		96 hrs.	-0.267	0.015	0.243	20.570
		168 hrs.	-0.297	0.017	0.245	19.049
		Total Percent Change	-10.20%	-21.86%	60.17%	-3.64%
FAB 3	15048	0 hrs.	-0.630	0.051	0.026	22.218
		96 hrs.	-0.632	0.046	0.043	21.762
		168 hrs.	-0.631	0.045	0.055	21.411
		Total Percent Change	0.16%	-14.77%	52.97%	-3.77%
EFETs						
FAB 2	14626	0 hrs.	-0.003	0.110	1.964	11.498
		96 hrs.	-0.007	0.108	2.073	11.574
		168 hrs.	0.004	0.102	3.574	10.560
		Total Percent Change	178.26%	-7.44%	45.06%	-8.88%
FAB 2	14759	0 hrs.	0.150	0.074	0.901	10.653
		96 hrs.	0.160	0.066	0.830	10.587
		168 hrs.	0.169	0.065	0.859	10.684
		Total Percent Change	11.41%	-13.74%	-4.99%	0.29%
FAB 3	14769	0 hrs.	-0.062	0.115	1.092	14.409
		96 hrs.	-0.047	0.080	5.165	10.701
		168 hrs.	-0.042	0.093	4.719	10.569
		Total Percent Change	-49.61%	-22.90%	76.87%	-36.33%
FAB 3	14939	0 hrs.	0.245	0.051	0.290	16.663
		96 hrs.	0.282	0.040	1.507	16.004
		168 hrs.	0.269	0.043	1.524	15.403
		Total Percent Change	9.06%	-18.62%	80.96%	-8.18%
FAB 3	15048	0 hrs.	0.013	0.071	0.064	19.257
		96 hrs.	0.004	0.070	0.179	18.371
		168 hrs.	0.008	0.074	0.244	16.902
		Total Percent Change	-61.72%	3.48%	73.66%	-13.93%

Table 7. Mean FET Parameters for Autoclaved Wafers						
Site	Run	Test Point	V _{th} (V)	I _d (mA/um)	I _g (nA/um)	BVGD (V)
DFETs						
FAB 2	14626	0 hrs.	-0.572	0.054	0.246	16.985
		48 hrs.	-0.566	0.054	0.295	16.687
		96 hrs.	-0.598	0.055	0.259	16.577
		Total Percent Change	4.36%	2.63%	5.10%	-2.46%
FAB 2	14759	0 hrs.	-0.541	0.049	0.164	17.133
		48 hrs.	-0.618	0.051	0.159	16.930
		96 hrs.	-0.544	0.049	0.171	16.953
		Total Percent Change	0.57%	-0.16%	3.74%	-1.06%
FAB 3	14769	0 hrs.	-0.703	0.071	0.228	19.526
		48 hrs.	-0.694	0.068	0.240	19.417
		96 hrs.	-0.695	0.068	0.220	19.407
		Total Percent Change	-1.04%	-3.87%	-3.88%	-0.61%
FAB 3	14939	0 hrs.	-0.387	0.025	0.135	19.160
		48 hrs.	-0.309	0.020	0.135	19.384
		96 hrs.	-0.356	0.021	0.128	19.352
		Total Percent Change	-8.61%	-17.66%	-5.45%	0.99%
FAB 3	15048	0 hrs.	-0.660	0.058	0.052	23.634
		48 hrs.	-0.637	0.061	0.078	21.662
		96 hrs.	-0.637	0.061	0.080	21.553
		Total Percent Change	-3.60%	4.02%	35.02%	-9.66%
EFETs						
FAB 2	14626	0 hrs.	0.027	0.101	1.947	11.309
		48 hrs.	0.029	0.102	2.291	11.072
		96 hrs.	0.017	0.103	2.236	10.970
		Total Percent Change	-59.40%	1.26%	12.91%	-3.09%
FAB 2	14759	0 hrs.	0.063	0.095	0.968	10.874
		48 hrs.	0.064	0.094	0.940	10.743
		96 hrs.	0.070	0.088	0.921	10.707
		Total Percent Change	9.69%	-7.95%	-5.11%	-1.56%
FAB 3	14769	0 hrs.	-0.066	0.113	0.863	14.909
		48 hrs.	-0.062	0.104	0.898	14.745
		96 hrs.	-0.062	0.103	0.881	14.519
		Total Percent Change	-7.88%	-9.23%	2.04%	-2.69%
FAB 3	14939	0 hrs.	0.201	0.055	0.406	13.825
		48 hrs.	0.227	0.038	0.457	14.397
		96 hrs.	0.224	0.038	0.446	14.453
		Total Percent Change	10.52%	-44.08%	8.92%	4.35%
FAB 3	15048	0 hrs.	-0.015	0.095	0.162	20.122
		48 hrs.	-0.008	0.089	0.171	18.997
		96 hrs.	-0.008	0.090	0.146	19.039
		Total Percent Change	-84.33%	-6.04%	-10.71%	-5.69%

Table 8. Mean FET Parameters for Temperature Cycled Wafers						
<i>Site</i>	<i>Run</i>	<i>Test Point</i>	<i>V_{th}</i> (V)	<i>I_d</i> (mA/um)	<i>I_g</i> (nA/um)	<i>BV_{GD}</i> (V)
DFETs						
FAB 2	14626	0 cycles	-0.618	0.073	0.267	17.285
		250 cycles	-0.573	0.056	0.245	16.491
		500 cycles	-0.578	0.055	0.272	16.382
		1000 cycles	-0.576	0.058	0.270	16.248
		Total Percent Change	-7.22%	-25.24%	1.04%	-6.38%
FAB 2	14759	0 cycles	-0.577	0.056	0.208	13.705
		250 cycles	-0.580	0.056	0.209	13.584
		500 cycles	-0.577	0.056	0.211	13.507
		Total Percent Change	-0.06%	1.06%	1.80%	-1.47%
FAB 3	14769	0 cycles	-0.698	0.070	0.230	20.228
		250 cycles	-0.687	0.068	0.233	20.123
		500 cycles	-0.711	0.069	0.226	20.018
		1000 cycles	-0.706	0.068	0.236	19.925
		Total Percent Change	1.21%	-1.78%	2.64%	-1.52%
FAB 3	14939	0 cycles	-0.396	0.028	0.115	19.380
		250 cycles	-0.392	0.027	0.083	19.463
		500 cycles	-0.399	0.028	0.083	19.209
		1000 cycles	-0.397	0.028	0.087	19.116
		Total Percent Change	0.28%	0.77%	-32.26%	-1.38%
FAB 3	15048	0 cycles	-0.589	0.054	0.193	20.284
		250 cycles	-0.587	0.058	0.187	19.980
		500 cycles	-0.579	0.057	0.185	19.934
		1000 cycles	-0.602	0.058	0.168	19.928
		Total Percent Change	2.15%	6.52%	-15.00%	-1.78%
EFETs						
FAB 2	14626	0 cycles	0.033	0.101	1.797	11.562
		250 cycles	0.032	0.103	1.892	11.430
		500 cycles	0.028	0.103	1.963	11.342
		1000 cycles	0.029	0.099	1.974	11.323
		Total Percent Change	-14.43%	-1.60%	8.97%	-2.12%
FAB 2	14759	0 cycles	0.060	0.095	1.182	10.778
		250 cycles	0.061	0.096	1.210	10.673
		500 cycles	0.061	0.096	1.198	10.589
		Total Percent Change	1.70%	1.26%	1.31%	-1.79%
FAB 3	14769	0 cycles	-0.074	0.114	0.714	14.714
		250 cycles	-0.073	0.113	0.661	14.585
		500 cycles	-0.074	0.112	0.668	14.489
		1000 cycles	-0.072	0.111	0.691	14.410
		Total Percent Change	-2.72%	-3.23%	-3.38%	-2.11%
FAB 3	14939	0 cycles	0.199	0.061	0.400	15.564
		250 cycles	0.198	0.061	0.250	15.745
		500 cycles	0.198	0.061	0.297	15.338
		1000 cycles	0.199	0.061	0.319	15.178
		Total Percent Change	0.09%	0.37%	-25.43%	-2.54%
FAB 3	15048	0 cycles	0.047	0.088	1.242	14.308
		250 cycles	0.051	0.094	1.376	14.146
		500 cycles	0.051	0.094	1.304	14.116
		1000 cycles	0.050	0.069	0.749	14.217
		Total Percent Change	5.81%	-26.67%	-65.88%	-0.64%

Summary

Overall, TriQuint's G7 process produces exceptional yield and reliability for the approximately 3,300 parameters tested per wafer before and after stressing. Most parameters stayed well within the guaranteed specification ranges. For parameters with reliability issues, i.e. Via3 and Ohmic to Metal0 contact chains, failure analysis and process improvements are on-going.