G16 Element Qualification Report
Revision 2

Purpose
This report summarizes element qualification test results obtained on TriQuint's G16 process fabricated at FAB 2 in Beaverton, OR and FAB 3 in Hillsboro, OR. A comprehensive series of testing was performed on wafer in order to verify successful transfer of the process to TriQuint's new facility in Hillsboro, OR.

Method
It was determined to use three runs from FAB 3, the new facility, for comparison with a baseline run from FAB 2. As of this writing, four runs from the two locations have completed testing. These runs and wafers are given in Table 1.

Table 1. Test Wafer Designation					
Process	*Location*	*Run*	*Air Bake Wafer*	*Autoclave Wafer*	*Temperature Cycle Wafer*
G16	FAB 2	12887	62711	62710	62709
G16	FAB 3	14951	75005	75003	75004
G16	FAB 3	13016	63834	63822	63818
G16	FAB 3	14821	73062	73065	73064

Stresses
Air Bake was performed for acceleration of thermally activated failure mechanisms. A temperature of 275ºC was chosen for maximum acceleration without compromising the dielectric material. Test points were at 0 hours, 96 hours and 168 hours.

Autoclave followed JEDEC Standard Number 22, Method A102-B. The purpose of this test was to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture to the wafer. The test condition consisted of 121ºC with a 100% relative humidity at two atmospheres. Test points were at 0 hours, 48 hours and 96 hours.

Temperature Cycle followed JEDEC Standard Number 22, Method A104-A, Condition "G." The purpose of this test was to determine the resistance of a wafer to alternating extremes of high and low temperatures. The test condition cycled at a low temperature of -40ºC to a high temperature of +125ºC. Test points were at 0 cycles, 250 cycles and 500 cycles.

Table 2 summarizes the stresses performed.

Table 2. Stress Parameters				
Test	*Test Condition*	*Test Point 1*	*Test Point 2*	*Test Point 3*
Air Bake	275ºC	0	96	168
Autoclave	121ºC, 100% RH	0	48	96
Temperature Cycle	-40ºC to +125ºC	0	250	500

The following were exceptions to the stresses above. FAB 2 Run 12887, Wafer 62709 was halted in temperature cycling after 480 cycles for cross-section comparison with early FAB 3 wafers. Wafer 62710 from the same run was tested after 24 and 72 hours autoclave in addition to test points at 0, 48 and 96 hours. Wafer 62711, also from Run 12887, was tested after 0, 24, 48 and 96 hours air bake. Attempts to retest the wafer after subsequent baking were unsuccessful due to prober contact issues; no 168 hour data was obtained.

FAB 3 Run 14951, Wafer 75003 was pulled from autoclave two hours early after a power outage, giving it a total time of 94 hours, rather than 96 hours. Wafer 75004 from the same run had contact problems at test after 500 temperature cycles. The wafer was continued in temperature cycle to 1000 cycles and retested.

Test Structures

Six sets of structures were chosen to be analyzed for the qualification report. Table 3 gives a general description of the structures used.

Table 3. Test Structures

Structure	*Structure Description*
FETs	0.6um x 50um gate with 1.0um gate to drain/source distance. DFET, EFET and GFET.
Vias/contact chains	Metal0 to Metal1, Metal1 to Metal2, MIM Metal to Metal1, Gate to Metal0, Gate to Metal1, NiCr to Metal0, Ohmic to Metal0 and Ohmic to Metal1. Via/contact chains with minimum dimension contacts.
Capacitors	25Kum^2, 50Kum^2, 100Kum^2, 200Kum^2, 400Kum^2 and 800Kum^2
Metals	Paired meanders, minimum width and pitch.
Combs	1.0um, 1.6um, 2.0um and 3.0um gaps, 1800um length. NiCr to NiCr, Gate to Gate, Ohmic to Ohmic, Metal0 to Metal0, MIM Metal to MIM Metal, Metal1 to Metal1, Gate to Ohmic. Also 0.6um, 0.7um, 0.8um, 0.9um, 1.0um, 1.2um, 1.4um, 1.6um, 1.8um, 2.0um gaps for FAB 2 and 1.6um, 1.8um, 2.0um for FAB 3; 1325um lengths.
Ohmic Contacts	2x2, 4, 8um implanted TLM with minimum length ohmic contacts.

Table 4 lists the electrical tests conducted on each of the structures.

Table 4. Electrical Tests

Structure	*Electrical Tests*				
FETs	Yield	Threshold Voltage	Drain Current	Gate Current	Breakdown Voltage
Vias/contact chains	Yield	Resistance			
Capacitors	Yield	Leakage at 10 and 15V			
Metals	Yield	Resistance			
Combs	Yield	Leakage at 10V			
Ohmic Contacts	Yield	Resistance			

Results

Capacitors

FAB 2 capacitors used an ET Nitride process producing better results both before and after stressing. Leakage values at 10V on all capacitor sizes were less than one nanoampere on FAB 2 wafers. The FAB 2 wafers also had only slightly higher leakage values at 20V. Yields on the 25Kum^2 capacitors were consistently 100% on all wafers. Yield decreased to ~70% on the 800Kum^2 capacitors.

FAB 3 capacitors used a Mattson Nitride process which caused low yield in capacitors. Leakage values were also higher than the FAB 2 ET Nitride capacitor results. Following these tests, G16 capacitors have reverted to the ET Nitride process for better yield and leakage values. Yield improvement efforts are on-going; ET Nitride will continue to be used until a comparable results Mattson Nitride process can be found.

Comb Structures

The general trend for FAB 3 and FAB 2 was a net decrease in leakage during air bake, autoclave and temperature cycle.

Table 5 gives the minimum reliably printable gap for a given layer combination in the two fabs. Note that the steppers used were *not* the same in the two fabs. For FAB 3, 1.6um was the minimum gap dimension measured, since this is well below the design rule minimums (2.0 or 3.0um, depending upon layer).

Table 5. Comb Structures

	FAB 3	*FAB 2*
Layer	Minimum Spacing	
Gate	1.6um	0.8um
Gate to Ohmic	1.6um	0.9um
Ohmic	1.6um	1.2um
Metal0	1.6um	0.8um
Metal1	1.6um	1.2um
MIM Metal	1.6um	1.2um
NiCr	1.6um	0.6um

Metals

Shorting noted on Metal0, Metal1 and Metal2 meanders on two of three FAB 3 runs significantly affected yield. The shorting issue is being addressed by process engineering. The resistance values for the three layers remained stable through all stresses, indicating no reliability issues.

Ohmic Contacts

Contact resistance was stable throughout autoclave and temperature cycling on all wafers. The FAB 2 air baked wafer showed an increase in ohmic contact resistance of almost 50%, from about 105 ohms (median value) to about 150 ohms. The FAB 3 wafers had higher initial contact resistance values (140 to 180 ohms, median values), but experienced little change due to baking.

Via/contact chains

Overall, via/contact chains from both fabs showed very little movement in resistance.

Two of three FAB 3 runs received an experimental ohmic alloy (AG heatpulse); the third FAB 3 run and the FAB 2 run received TriQuint's standard ohmic alloy. Ohmic to Metal1 and Ohmic to Metal0 chains decreased in resistance during autoclave and temperature cycle on all four runs.

Ohmic to Metal1 and Ohmic to Metal0 chains decreased in resistance during air bake on the two wafers that received the standard ohmic alloy. On the two baked wafers that received the experimental ohmic alloy, Ohmic to Metal0 via chains showed a large increase in per via resistance, from about 2 ohms to 6 ohms. The Ohmic to Metal1 via/contact chain resistances on Wafer 75005 increased a much smaller amount (<20%) and the Ohmic to Metal1 via/contact chain resistance on Wafer 73062 decreased in resistance after baking. All other via/contact chains were largely stable; typical resistance increases on the four baked wafers were on the order of a few percent.

Sixteen Via/contact chain failures were located. Table 6 gives a description of which vias failed. Thirteen of the 16 received autoclave stressing. Twelve of the 16 were Metal1 to Metal2 vias. Eleven of the 16 were edge tiles on the wafer; non-edge tiles are highlighted. Of the non-edge tiles, all are Metal1 to Metal2 via strings, four of five of which opened in autoclave. (Note that there are a total of 130 separate Metal1 to Metal2 via strings analyzed on EACH wafer.)

Table 6. G16 Via/Contact Chain Failure Description

Location	Run	Wafer #	Stress	Test #	Site #	Structure Description
FAB 2	12887	62711	Air Bake	1503	17	Metal1 to Metal2, 30um wide lines, 48 3.0x3.0um min vias with 17um lines
FAB 2	12887	62710	Autoclave	100	23	Metal0 to Metal1, 3200 2.0x2.0um vias max density
FAB 3	13016	63822	Autoclave	1100	5, 23, **24**	Metal1 to Metal2, 300x30um lines, 48 3.0x3.0um min vias
FAB 3	13016	63822	Autoclave	1503	**24**	Metal1 to Metal2, 30um wide lines, 48 3.0x3.0um min vias with 17um lines
FAB 3	13016	63818	Temp Cycle	1503	3, **6**	Metal1 to Metal2, 30um wide lines, 48 3.0x3.0um min vias with 17um lines
FAB 3	14821	73065	Autoclave	300	**24**, **25**	Metal1 to Metal2, 3200 2.0x2.0um vias max density
FAB 3	14821	73065	Autoclave	1601	5	Metal0 to Metal1, 300um lines, 24 2.0x2.0um min vias with 30um lines
FAB 3	14821	73065	Autoclave	1703	4	Metal1 to Metal2, 300um lines, 24 3.0x3.0um min vias with 5um lines
FAB 3	14951	75003	Autoclave	300	26	Metal1 to Metal2, 3200 2.0x2.0um vias max density
FAB 3	14951	75003	Autoclave	400	26	MIM Metal to Metal1, 3200 2.0x2.0um vias max density
FAB 3	14951	75003	Autoclave	700	26	NiCr to Metal0, 3200 vias max density, 2.0um NiCr and 3.0um Metal0 with 2.0um overlap
FAB 3	14951	75003	Autoclave	1503	11	Metal1 to Metal2, 30um wide lines, 48 3.0x3.0um min vias with 17um lines

The majority of the via/contact chain failures occurred on metal 1 to metal 2 (upper level) via chains in autoclave, as noted above. Our most similar process, G7 (QEDA2), also experienced similar via chain opens following autoclave, largely on two of five runs tested. Since there were a larger number of opens on the G7 material, we chose to proceed with failure analysis on this material. The major difference between the two processes is in the minimum via dimensions (1x4 on G7 and 3x3 on G16). The upper level via chains tested electrically open on G7 and G16 wafers following 48 or 96 hours autoclave (121C, 100% relative humidity). The chains were manually probed to verify the automated test. One G7 wafer was cleaved, and random vias examined by scanning electron microscopy (SEM). All of the cleaved vias randomly examined showed good adhesion, with characteristic necking through the center of the via due to the cleave.

A second G7 wafer was stripped of passivation, and ILD etched back to expose metal 2. The chains were manually probed again to verify the opens. Manual probing was then continued to identify individual pairs of open vias within a chain.

In all cases, via pairs that could be identified as containing an open were found to be located on the outside edges of the rectangular arrays of vias. No more than one or two pairs of vias per

chain could be identified as containing an open. Two of the via pairs identified as containing an open were cross-sectioned using focused ion beam (FIB) micromachining. An additional pair of vias from the center of one of the two chains was also cross-sectioned.

FIB cross-sections showed **no** fractures or voids, and the vias were well-formed. Comparison of the open vias with vias from the center of the chain showed no obvious differences between the vias except for a 'thicker' adhesion layer on the open vias, with a qualitatively different appearance. Note that the difference in appearance of the adhesion layers was the same regardless of whether the layer was located in the conduction path (at the base of the via), or outside the conduction path (under the connecting metal lines).

Auger analysis was attempted on the cross-sectioned part, but was unsuccessful due to the "box" nature of the FIB cut.

Failure is currently attributed to oxidation of the adhesion layer during moisture stressing. The unique location of the affected vias indicates an issue with moisture penetration through the nitride passivation seal, most likely due to planarization effects at the edge of a dense feature (the chain itself). Experiments directed at improving the effectiveness of the passivation layer as a moisture barrier and at increasing the moisture resistance of the adhesion layer are ongoing.

FETs

Most FET parameters remained stable through all three stresses, staying well within guaranteed specification ranges. Threshold voltage and drain current of the FAB 2 EFETs had prober difficulties and no data was collected. Mean values of FET parameters during stressing are given in Tables 8-10. Three FET failures were found overall. Table 7 below gives a description of which FETs failed. Two of the three are likely attributable to their location on the wafer -- sites 3 and 5 are both edge tiles. However, failure analysis on the FETs has so far been inconclusive.

Table 7. G16 FET Failure Description

Location	*Run*	*Wafer #*	*Stress*	*Test #*	*Site #*	*Structure Description*
FAB 3	14821	73065	Autoclave	3124	3	0.6x50um gate with 1.0um gate to drain/source distance EFET
FAB 3	14951	75005	Air Bake	2621	5	0.6x50um gate with 1.0um gate to drain/source distance EFET
FAB 3	14951	75003	Autoclave	3100, 3124	20	0.6x50um gate with 1.0um gate to drain/source distance EFET

Table 8. Mean FET Parameters for Air Baked Wafers						
Site	*Run*	*Test Point*	*Vth (V)*	*Id (mA/um)*	*Ig (nA/um)*	*BVGD (V)*
DFETs						
FAB 2	12887	0 hrs.	-0.574	0.061	14.442	11.554
		96 hrs.	-0.571	0.059	14.442	11.560
		Total Percent Change	0.56%	-4.03%	0.00%	0.05%
FAB 3	14951	0 hrs.	-0.482	0.046	17.406	13.134
		96 hrs.	-0.460	0.041	41.346	10.007
		168 hrs.	-0.475	0.044	27.652	11.743
		Total Percent Change	1.60%	-4.67%	37.05%	-11.85%
FAB 3	13016	0 hrs.	-0.564	0.060	29.012	12.406
		96 hrs.	-0.555	0.058	17.044	13.585
		168 hrs.	-0.550	0.058	11.439	13.090
		Total Percent Change	2.47%	-4.29%	-153.63%	5.22%
FAB 3	14821	0 hrs.	-0.580	0.062	8.425	13.022
		96 hrs.	-0.642	0.066	31.212	9.504
		168 hrs.	-0.637	0.065	30.588	8.619
		Total Percent Change	-8.92%	4.59%	72.46%	-51.09%
EFETs						
FAB 2	12887	0 hrs.	N/A	N/A	1.361	20.296
		96 hrs.	N/A	N/A	1.346	20.286
		Total Percent Change	N/A	N/A	-1.10%	-0.05%
FAB 3	14951	0 hrs.	0.231	0.057	3.021	16.886
		96 hrs.	0.274	0.046	8.613	15.752
		168 hrs.	0.267	0.050	7.526	15.656
		Total Percent Change	13.48%	-15.1%	59.9%	-7.86%
FAB 3	13016	0 hrs.	0.207	0.065	5.441	14.796
		96 hrs.	0.207	0.064	11.048	14.239
		168 hrs.	0.208	0.063	9.499	13.948
		Total Percent Change	0.66%	-2.78%	42.72%	-6.07%
FAB 3	14821	0 hrs.	0.157	0.070	0.980	17.206
		96 hrs.	0.181	0.062	6.043	13.860
		168 hrs.	0.182	0.061	6.341	13.103
		Total Percent Change	13.83%	-14.76%	84.55%	-31.31%
GFETs						
FAB 2	12887	0 hrs.	-2.084	0.262	9.983	11.713
		96 hrs.	-2.078	0.255	9.753	11.882
		Total Percent Change	0.31%	-2.50%	-2.37%	1.42%
FAB 3	14951	0 hrs.	-1.952	0.232	10.372	14.150
		96 hrs.	-2.040	0.241	16.276	11.757
		168 hrs.	-2.048	0.240	22.164	12.243
		Total Percent Change	-4.71%	3.31%	53.20%	-15.57%
FAB 3	13016	0 hrs.	-2.114	0.256	10.241	13.772
		96 hrs.	-2.095	0.254	11.773	14.122
		168 hrs.	-2.085	0.254	8.942	13.171
		Total Percent Change	1.41%	-1.10%	-14.52%	-4.56%
FAB 3	14821	0 hrs.	-2.005	0.237	7.508	13.962
		96 hrs.	-2.244	0.246	27.800	9.996
		168 hrs.	-2.257	0.241	30.682	8.812
		Total Percent Change	-11.18%	1.75%	75.53%	-58.45%

Table 9. Mean FET Parameters for Autoclaved Wafers						
Site	Run	Test Point	Vth (V)	Id (mA/um)	Ig (nA/um)	BVGD (V)
DFETs						
FAB 2	12887	0 hrs.	-0.549	0.057	11.967	12.198
		48 hrs.	-0.553	0.057	8.268	12.361
		96 hrs.	-0.553	0.057	7.737	12.245
		Total Percent Change	-0.72%	0.00%	-54.67%	0.38%
FAB 3	14951	0 hrs.	-0.541	0.055	18.720	13.111
		48 hrs.	-0.531	0.053	14.280	12.607
		96 hrs.	-0.534	0.053	12.917	12.524
		Total Percent Change	1.31%	-3.77%	-44.93%	-4.69%
FAB 3	13016	0 hrs.	-0.587	0.064	35.644	12.866
		48 hrs.	-0.589	0.064	28.916	13.119
		96 hrs.	-0.588	0.064	28.264	13.077
		Total Percent Change	-0.07%	0.22%	-26.11%	1.61%
FAB 3	14821	0 hrs.	-0.638	0.073	10.907	13.080
		48 hrs.	-0.634	0.071	9.530	13.082
		96 hrs.	-0.637	0.071	5.710	13.636
		Total Percent Change	0.13%	-3.50%	-91.01%	4.07%
EFETs						
FAB 2	12887	0 hrs.	N/A	N/A	1.375	20.373
		48 hrs.	N/A	N/A	0.764	20.377
		96 hrs.	N/A	N/A	0.763	20.162
		Total Percent Change	N/A	N/A	-80.12%	-1.05%
FAB 3	14951	0 hrs.	0.189	0.067	3.389	15.353
		48 hrs.	0.201	0.061	3.568	15.752
		96 hrs.	0.203	0.061	3.993	14.406
		Total Percent Change	6.90%	-9.12%	15.13%	-6.57%
FAB 3	13016	0 hrs.	0.206	0.064	13.718	13.304
		48 hrs.	0.209	0.061	13.577	13.617
		96 hrs.	0.210	0.062	14.984	13.514
		Total Percent Change	1.95%	-4.37%	8.45%	1.55%
FAB 3	14821	0 hrs.	0.131	0.071	1.401	18.818
		48 hrs.	0.135	0.063	1.431	18.863
		96 hrs.	0.148	0.063	0.768	18.722
		Total Percent Change	11.00%	-12.83%	-82.35%	-0.52%
GFETs						
FAB 3	12887	0 hrs.	-2.085	0.261	10.937	12.303
		48 hrs.	-2.058	0.259	8.620	12.540
		96 hrs.	-2.055	0.257	8.203	12.510
		Total Percent Change	1.46%	-1.56%	-33.33%	1.65%
FAB 3	14951	0 hrs.	-2.040	0.246	11.980	14.063
		48 hrs.	-2.046	0.245	13.294	13.581
		96 hrs.	-2.042	0.245	12.608	13.526
		Total Percent Change	-0.13%	-0.51%	4.98%	-3.97%
FAB 3	13016	0 hrs.	-2.157	0.264	14.457	14.051
		48 hrs.	-2.159	0.264	16.328	14.127
		96 hrs.	-2.160	0.265	15.875	14.014
		Total Percent Change	-0.13%	0.23%	8.93%	-0.26%
FAB 3	14821	0 hrs.	-2.169	0.264	9.520	13.984
		48 hrs.	-2.172	0.263	5.462	14.406
		96 hrs.	-2.142	0.259	3.667	14.569
		Total Percent Change	1.29%	-1.87%	-159.65%	4.01%

Table 10. Mean FET Parameters for Temperature Cycled Wafers						
Site	*Run*	*Test Point*	*Vth (V)*	*Id (mA/um)*	*Ig (nA/um)*	*BVGD (V)*
DFETs						
FAB 2	12887	0 cycles	-0.593	0.062	13.384	11.759
		500 cycles	-0.592	0.063	11.929	11.872
		Total Percent Change	0.03%	1.65%	-12.20%	0.95%
FAB 3	14951	0 cycles	-0.516	0.052	18.584	10.672
		250 cycles	-0.517	0.052	17.221	10.544
		500 cycles	-0.517	0.052	17.783	10.495
		Total Percent Change	-0.12%	-0.26%	-4.50%	-1.68%
FAB 3	13016	0 cycles	-0.619	0.072	36.716	12.436
		250 cycles	-0.614	0.069	33.068	12.291
		500 cycles	-0.617	0.069	29.708	12.146
		Total Percent Change	0.32%	-3.19%	-23.59%	-2.39%
FAB 3	14821	0 cycles	-0.663	0.079	7.228	13.134
		250 cycles	-0.660	0.077	7.120	12.866
		500 cycles	-0.666	0.077	6.526	12.799
		Total Percent Change	-0.33%	-2.54%	-10.76%	-2.62%
EFETs						
FAB 2	12887	0 cycles	N/A	N/A	1.394	21.018
		500 cycles	N/A	N/A	1.060	21.265
		Total Percent Change	N/A	N/A	-31.49%	1.16%
FAB 3	14951	0 cycles	0.193	0.068	8.226	10.288
		250 cycles	0.194	0.068	4.915	10.210
		500 cycles	0.194	0.068	5.483	10.166
		Total Percent Change	0.54%	-0.13%	-50.04%	-1.20%
FAB 3	13016	0 cycles	0.187	0.070	13.308	13.494
		250 cycles	0.189	0.069	11.652	13.367
		500 cycles	0.188	0.069	10.213	13.264
		Total Percent Change	0.47%	-1.88%	-30.31%	-1.74%
FAB 3	14821	0 cycles	0.138	0.080	0.899	18.898
		250 cycles	0.145	0.073	0.764	18.492
		500 cycles	0.145	0.073	0.748	18.341
		Total Percent Change	5.01%	-9.96%	-20.18%	-3.04%
GFETs						
FAB 2	12887	0 cycles	-2.103	0.266	8.906	11.885
		500 cycles	-2.101	0.266	8.627	12.035
		Total Percent Change	0.11%	0.18%	-3.24%	1.25%
FAB 3	14951	0 cycles	-2.009	0.239	12.831	12.888
		250 cycles	-2.017	0.240	12.137	12.620
		500 cycles	-2.023	0.241	12.238	12.520
		Total Percent Change	-0.71%	0.50%	-4.84%	-2.95%
FAB 3	13016	0 cycles	-2.203	0.267	18.141	13.399
		250 cycles	-2.209	0.267	17.641	13.158
		500 cycles	-2.210	0.267	17.073	12.969
		Total Percent Change	-0.33%	0.06%	-6.26%	-3.32%
FAB 3	14821	0 cycles	-2.112	0.253	5.891	15.357
		250 cycles	-2.103	0.251	5.117	15.183
		500 cycles	-2.102	0.251	4.637	15.054
		Total Percent Change	0.46%	-0.86%	-27.03%	-2.01%

Summary:

Triquint is satisfied based on the data collected that the material produced in the new facility compares favorably with the material from the Beaverton facility. Some early FAB 3 material experienced larger parameter shifts than the corresponding Beaverton material; however, the differences have largely disappeared as the processes have matured at the new facility.