



G02 Element Qualification Report Revision 2

Purpose

This report summarizes element qualification test results obtained on TriQuint's G02 process fabricated at FAB 2 in Beaverton, OR and FAB 3 in Hillsboro, OR. A comprehensive series of testing was performed on wafer in order to verify successful transfer of the process to TriQuint's new facility in Hillsboro, OR.

Method

It was determined to use three runs from FAB 3, the new facility, for comparison with a baseline run from FAB 2. As of this writing, all runs have completed testing. The wafers and runs are given in Table 1.

Table 1. Test Wafer Designation					
<i>Process</i>	<i>Location</i>	<i>Run</i>	<i>Air Bake Wafer</i>	<i>Autoclave Wafer</i>	<i>Temperature Cycle Wafer</i>
G02	FAB 2	15326	82851	82848	82849
G02	FAB 3	15085	78691	78695	78699
G02	FAB 3	15059	88509	88511	88513
G02	FAB 3	15206	79361	79363	79367

Stresses

Air Bake was performed for acceleration of thermally activated failure mechanisms. A temperature of 275°C was chosen for maximum acceleration without compromising the dielectric material. Test points were at 0 hours, 96 hours and 168 hours.

Autoclave followed JEDEC Standard Number 22, Method A102-B. The purpose of this test was to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture to the wafer. The test condition consisted of 121°C with a 100% relative humidity at two atmospheres. Test points were at 0 hours, 48 hours and 96 hours.

Temperature Cycle followed JEDEC Standard Number 22, Method A104-A, Condition "G." The purpose of this test was to determine the resistance of a wafer to alternating extremes of high and low temperatures. The test condition cycled at a low temperature of -40°C to a high temperature of +125°C. Test points were at 0 cycles, 250 cycles and 500 cycles.

Table 2 summarizes the stresses performed.

Table 2. Stress Parameters				
<i>Test</i>	<i>Test Condition</i>	<i>Test Point 1</i>	<i>Test Point 2</i>	<i>Test Point 3</i>
Air Bake	275°C	0	96	168
Autoclave	121°C, 100% RH	0	48	96
Temperature Cycle	-40°C to +125°C	0	250	500

Test Structures

Six sets of structures were chosen to be analyzed for the qualification report. Table 3 gives a general description of the structures used.

<i>Structure</i>	<i>Structure Description</i>
FETs	0.7um x 50um gate with 1.0um gate to drain/source distance. DFET, EFET.
Vias/contact chains	Gate to Ohmic, Metal0 to Air Bridge, Ohmic to Air Bridge, Gate to Air Bridge, Ohmic to Metal0 and NiCr to Metal0. Via/contact chains with minimum dimension contacts.
Capacitors	25Kum ² , 50Kum ² , 100Kum ² , 200Kum ² , 400Kum ² and 800Kum ²
Metals	Paired meanders, minimum width and pitch.
Combs	1.0um, 1.6um, 2.0um and 3.0um gaps, 1800um length. NiCr to NiCr, Gate to Gate, Ohmic to Ohmic, Metal0 to Metal0, Ohmic to N+, Gate to Ohmic and Air Bridge to Air Bridge. Also 0.6um, 0.7um, 0.8um, 0.9um, 1.0um, 1.2um, 1.4um, 1.6um, 1.8um, 2.0um gaps, 1325um length.
Ohmic Contacts	2x2, 4, 8um implanted TLM with minimum length ohmic contacts.

Table 4 lists the electrical tests conducted on each of the structures.

<i>Structure</i>	<i>Electrical Tests</i>					
FETs	Yield	Threshold Voltage	Drain Current	Transconductance	Gate Current	Breakdown Voltage
Vias/contact chains	Yield	Resistance				
Capacitors	Yield	Leakage at 10 and 25V				
Metals	Yield	Resistance				
Combs	Yield	Leakage at 10V				
Ohmic Contacts	Yield	Resistance				

Results

FETs

Run 15206 had E and DFETs with lower than acceptable V_{th} values at initial test, as did one wafer from run 15326 (DFETs). It was decided to use these wafers for reliability stressing in spite of the negative threshold voltages.

FET parameters of autoclaved and temperature cycled wafers from both fabs were very stable. With the exception of the FET threshold voltages noted above (negative at initial test), all parameters stayed well within the guaranteed specification limits. Although some of the gate leakage current values showed large percentage changes, the absolute values stayed consistently in the nanoamp per micron range.

Baked wafers experienced positive shifts in threshold voltage, and in two cases, the shift pushed DFETs out of the guaranteed specification range -- to -444 and -438 mV vs. a maximum specification of -450 mV. These represent values less than 3% above the maximum specification value. Because the three FAB 3 runs showed decreasing percentage and absolute shifts in DFET V_{th} as the process matured at the new facility, this is believed not to be an issue. All other FET parameters remained within the guaranteed specification limits. As noted above for TriQuint Semiconductor, Inc. • 2300 N.E. Brookwood Pkwy. • Hillsboro, OR 97124 • 503-615-9000

autoclaved and temperature cycled wafers, some of the gate leakage current values showed large percentage changes, but the absolute values stayed consistently in the nanoamp per micron range. Decreases in drain current, breakdown voltage and transconductance over 168 hours at 275C were in some cases greater than the targeted 20%. However, with the exception of the DFET threshold voltages noted, the values remained within specification limits.

Mean values of FET parameters during stressing are given in Tables 5-7.

Table 5. Mean FET Parameters for Autoclaved Wafers							
<i>Site</i>	<i>Run</i>	<i>Test Point</i>	<i>V_{th}</i> (V)	<i>I_{max}</i> (mA)	<i>G_m</i> (mS/mm)	<i>I_g</i> (nA/um)	<i>BVGD</i> (V)
DFETs							
FAB 2	15326	0 hrs.	-0.772	9.95	6.97	1.188	16.48
		48 hrs.	-0.77	9.92	6.95	3.27	16.75
		96 hrs.	-0.772	9.64	6.79	1.188	16.61
		Total Percent Change	0.00%	-3.12%	-2.58%	0.00%	0.79%
FAB 3	15059	0 hrs.	-0.54	7.79	5.47	2.77	11.42
		48 hrs.	-0.573	7.74	5.37	4.72	12.32
		96 hrs.	-0.565	7.73	5.4	0.4	12.06
		Total Percent Change	-4.63%	-0.77%	-1.28%	-85.56%	5.60%
	15085	0 hrs.	-0.563	8.4	5.95	2.92	14.47
		48 hrs.	-0.562	8.38	5.84	1.77	14.44
		96 hrs.	-0.562	8.39	5.8	4.85	14.47
		Total Percent Change	0.18%	-0.12%	-2.52%	66.10%	0.00%
	15206	0 hrs.	-0.911	10.80	7.26	2.77	15.54
		48 hrs.	-0.915	10.83	7.25	2.92	15.64
		96 hrs.	-0.916	10.83	7.25	3.61	15.69
		Total Percent Change	-0.55%	0.29%	-0.08%	30.56%	1.02%
EFETs							
FAB 2	15326	0 hrs.	0.05	3.86	7.05	0.25	21.96
		48 hrs.	0.045	3.87	7.05	2.36	22.01
		96 hrs.	0.027	3.22	6.59	1	22.09
		Total Percent Change	-46.00%	-16.58%	-6.52%	300.00%	0.59%
FAB 3	15059	0 hrs.	0.179	2.61	5.05	1.85	14.06
		48 hrs.	0.176	2.62	5.07	4.15	14.28
		96 hrs.	0.17	2.63	5.06	5.38	14.39
		Total Percent Change	-5.03%	0.77%	0.20%	190.81%	2.35%
	15085	0 hrs.	0.169	2.86	5.61	3	16.81
		48 hrs.	0.17	2.85	5.59	1.23	16.82
		96 hrs.	0.169	2.85	5.59	4.38	16.87
		Total Percent Change	0.00%	-0.35%	-0.36%	46.00%	0.36%
	15206	0 hrs.	-.040	4.45	7.60	2.23	19.55
		48 hrs.	-.080	4.47	7.61	1.92	19.59
		96 hrs.	-.082	4.47	7.61	3.44	19.63
		Total Percent Change	-104.6%	0.50%	0.09%	54.26%	0.41%

Table 6. Mean FET Parameters for Temperature Cycled Wafers							
<i>Site</i>	<i>Run</i>	<i>Test Point</i>	<i>V_{th}</i> (V)	<i>I_{max}</i> (mA)	<i>G_m</i> (mS/mm)	<i>I_g</i> (nA/um)	<i>BV_{GD}</i> (V)
DFETs							
FAB 3	15059	0 cycles	-0.589	8.4	5.93	3.33	13.93
		250 cycles	-0.591	8.23	5.85	1.38	13.88
		500 cycles	-0.594	8.28	5.86	2.62	13.95
		Total Percent Change	-0.85%	-1.43%	-1.18%	-21.32%	0.14%
	15085	0 cycles	-0.543	8.37	5.96	3.85	14.79
		250 cycles	-0.542	8.36	5.91	2.62	14.73
		500 cycles	-0.544	8.36	5.95	2.77	14.76
		Total Percent Change	-0.18%	-0.12%	-0.17%	-28.05%	-0.20%
	15206	0 cycles	-.952	11.24	7.49	2.38	13.89
		250 cycles	-.956	11.26	7.49	2.77	13.99
		500 cycles	-.958	11.28	7.50	1.15	14.03
		Total Percent Change	5.25%	0.30%	0.01%	-51.61%	0.95%
EFETs							
FAB 3	15059	0 cycles	0.18	2.79	5.41	2.5	16.77
		250 cycles	0.171	2.63	5.11	1.76	15.72
		500 cycles	0.169	2.64	5.12	2.16	15.78
		Total Percent Change	-6.11%	-5.38%	-5.36%	-13.60%	-5.90%
	15085	0 cycles	0.185	2.79	5.5	4.23	17.92
		250 cycles	0.186	2.78	5.48	1.38	17.9
		500 cycles	0.186	2.78	5.48	2	17.93
		Total Percent Change	0.54%	-0.36%	-0.36%	-52.72%	0.06%
	15206	0 cycles	-.056	4.65	7.86	1.46	19.76
		250 cycles	-.059	4.67	7.86	2.46	19.85
		500 cycles	-.060	4.68	7.87	1.61	19.91
		Total Percent Change	-5.53%	0.57%	0.12%	10.53%	0.74%

Table 7. Mean FET Parameters for Air Baked Wafers							
Site	Run	Test Point	V _{th} (V)	I _{max} (mA)	G _m (mS/mm)	I _g (nA/um)	BVGD (V)
DFETs							
FAB 2	15326	0 hrs.	-0.672	9.24	6.56		16.29
		96 hrs.	-0.625	8.91	6.47		
		168 hrs.	-0.604	8.76	6.38		15.43
		Total Percent Change	10.12%	-5.19%	-2.74%	24.70%	-5.28%
FAB 3	15059	0 hrs.	-0.658	8.76	6.18	2.9	12.2
		96 hrs.	-0.448	7.24	5.2		9.72
		168 hrs.	-0.444	6.56	4.74	37.4	9.33
		Total Percent Change	32.52%	-25.11%	-23.30%	1189.66%	-23.52%
	15085	0 hrs.	-0.517	8.03	5.61	2.9	13.9
		96 hrs.	-0.465	7.25	5.06	2.8	10.3
		168 hrs.	-0.438	6.95	4.82	9	10.1
		Total Percent Change	15.28%	-13.45%	-14.08%	210.34%	-27.34%
	15206	0 hrs.	-0.917	10.84	7.27	1.08	16.06
		96 hrs.	-0.886	10.20	6.89	1.54	17.16
		168 hrs.	-0.860	9.59	6.39	3.38	17.02
		Total Percent Change	6.22%	-11.54%	-12.04%	226.86%	6.00%
EFETs							
FAB 2	15326	0 hrs.	0.106	3.43	6.68	3.3	21.5
		96 hrs.	0.129	3.21	6.54		
		168 hrs.	0.142	3.15	6.34	1.1	20.1
		Total Percent Change	33.96%	-8.16%	-5.09%	-66.67%	-6.51%
FAB 3	15059	0 hrs.	0.0921	3.19	6.03	2.3	14.79
		96 hrs.	0.204	2.32	4.52		12.59
		168 hrs.	0.241	1.97	3.87	4.4	12.25
		Total Percent Change	161.67%	-38.24%	-35.82%	91.30%	-17.17%
	15085	0 hrs.	0.203	2.6	5.04	2.7	16.3
		96 hrs.	0.258	2.02	3.76	2.3	14.3
		168 hrs.	0.279	1.84	3.33	4.2	14.1
		Total Percent Change	37.44%	-29.23%	-33.93%	55.56%	-13.50%
	15206	0 hrs.	-.043	4.49	7.63	1.77	20.59
		96 hrs.	.001	4.00	7.06	3.25	21.39
		168 hrs.	.019	3.62	6.45	3.24	21.51
		Total Percent Change	142.83%	-19.33%	-15.54%	83.02%	4.48%

Comb Structures

The general trend for FAB 3 and FAB 2 was a net decrease in leakage during air bake, autoclave and temperature cycle.

Table 8 gives the minimum reliably printable gap for a given layer combination in the two fabs. Note that the steppers used were *not* the same in the two fabs.

	<i>FAB 3</i>	<i>FAB 2</i>
<i>Layer</i>	Minimum Spacing	
Gate to Gate	0.7um	0.6um
Gate to Ohmic	1.0um	0.9um
Ohmic	1.2um	1.0um
Ohmic/Implant	1.2um	1.2um
NiCr	0.7um	0.6um
Metal0	0.7um	0.6um
Landed Air Bridge	1.6um	1.2um

Metals

Run 15206 had problems with NiCr metal during processing. It was decided to use the run for reliability testing, but to eliminate the NiCr tests for this run only.

Metal line resistance values were stable during both autoclave and temperature cycling, with the exception of ohmic metal which decreased in resistance by about 6-9% under both stresses.

The baked FAB 2 wafer showed a similar drop in ohmic resistance to the autoclaved and temperature cycled wafers; ohmic metal resistance was stable on the baked FAB 3 wafers. NiCr metal resistance was stable during bake on all wafers included in the test. Gate, metal 0 and air bridge metals all showed small increases in resistance during bake. These changes were on the order of 3-10% for gate metal and 6-15% for air bridge lines. Metal 0 lines increased by about 3% on the FAB 2 wafer, compared with about 20% for the FAB 3 wafers.

Ohmic Contacts

Contact resistance was stable throughout autoclave and temperature cycling on all wafers.

FAB 3 baked wafers showed an increase in ohmic contact resistance of 42-44% compared with an increase of 15% for the FAB 2 baked wafer; however, both the initial and final contact resistances of the FAB 3 wafers were lower than the corresponding values for the FAB 2 wafer.

Capacitors

Capacitors showed little to no changes in leakage current over all stresses.

Via/contact chains

Autoclaved and temperature cycled via/contact chains from both fabs showed very little movement in resistance. The largest changes occurred on FAB 2 autoclaved material, where Metal 0 to air bridge and gate to air bridge chains showed increases of 8% and 13% respectively over 96 hours, compared with $\leq 2\%$ for the FAB 3 wafers. Ohmic to air bridge and Ohmic to Metal 0 chains decreased in resistance during autoclave and temperature cycle, and gate to Metal 0 and NiCr to Metal 0 chains were largely stable.

On the baked wafers, gate to Metal 0 contact chains showed a slight increase for FAB 2 compared with an increase of about 16% for FAB 3 over 168 hours. Gate to air bridge chains increased about 7% for the FAB 2 wafer, and about 28% for the FAB 3 wafers. Metal 0 to air bridge via chains increased on all wafers, but the largest increase was for FAB 3 run 15085 (32%). NiCr to Metal 0 contact chains were stable on all wafers. Ohmic to Metal 0 chains increased about 28% on the FAB 2 wafer, and decreased on FAB 3 wafers. Ohmic to air bridge

chains were stable in FAB 2; the same chains in FAB 3 showed a net decrease in resistance on one wafer (run 15059), and an increase of about 38% on another (run 15085), and a increase in the spread of values on run 15206, with a slight decrease in the median value.

Summary

Overall, TriQuint feels that the G02 (QEDA) process in the new facility compares favorably with the same process in FAB 2. FETs, via/contact chains, combs, metals, capacitors and ohmic contacts all appear to be robust to autoclave, temperature cycling and air bake.