

Process Qualification

Qualification of the 100mm HBT Process

Abstract

This report summarizes the reliability tests performed to qualify TriQuint Semiconductor's HBT GaAs wafer fabrication process on 100mm Wafers.

Wafer Level Reliability Testing:

On-wafer process control monitor (PCM) structures representative of circuit elements.

Product Level Reliability Testing:

Two representative product test vehicles were selected for this qualification.

•Qualification Vehicles:

- TQ7132 - A CDMA Cell Phone Power Amplifier.
- TQ7125 - A TDMA Cell Phone Power Amplifier.

*The TQ7132 was packaged in a 4X4-16 QFN style package.
The TQ-7125 was packaged in a 3X3-16 QFN style package.
Both products were packaged by subcontractor C.*

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Process Description

TriQuint's InGaP HBT process is a Gallium Arsenide (GaAs) semiconductor process fabricated at TriQuint's Oregon facility. The process uses epitaxial layers grown on GaAs wafers to support Heterjunction Bipolar Junction Transistor (HBT) active devices. The HBT process includes Nichrome (NiCr) resistors, silicon nitride MIM capacitors, 2 levels of global interconnect, and substrate via holes.

Wafer Level Reliability Testing:

The vehicle for wafer-level reliability evaluation was the on-wafer process control monitor (PCM) structures. The PCM structures are representative of the various passive and active components manufactured with the HBT process. These structures include individual active devices, capacitors, various via and contact chains, leakage combs and other proprietary structures.

Product Level Reliability Testing

TQ7132 - Cell Phone Power Amplifier

The TQ7132 is a two stage, 3 Volt HBT power amplifier die designed for use in CDMA handsets operating in the US cellular frequency band. The TQ7132 die is 4 mils thick and utilizes via's for ground contact the backside of the die. The TQ7132 has an external quiescent current control function which allows the user to reduce the device bias current during low transmit power times, thus extending battery life and talk time.

TQ7125 - Cell Phone Power Amplifier

The TQ7125 is a 3.5-volt HBT Power Amplifier RFIC intended for use in TDMA cellular applications. The circuit is a two-stage class AB power amplifier with internally stabilized, closed-loop bias circuitry for each of the two stages. The TQ7125 has high/low power modes. The low power setting reduces the second stage quiescent current, allowing higher efficiency operation for lower output power TDMA operation, as well as higher efficiency for full power AMPS operation.

Test Plan:**Table 1. Wafer Level Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
Environmental	1. High Temperature Unbiased Bake	Determine the effect of High Temperature Storage.	275°C Air Bake 168 hrs	3 Lots 1 Wafer/Lot
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 1 Wafer/Lot
	3. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 500 Cycles	3 Lots 1 Wafer/Lot

Table 2. Product Level Qualification Test Plan.

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
HTOL	1. Bias Life test	Determine the effect of bias and temp on the device over time.	1,000 hrs @ Bias & Ambient Temp. conditions adjusted to raise the Junction Temp. to ~150°C	3 Lots 77 (1)
Environmental	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	3 Lots 160 (1)
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 77 (1)
	3. HAST	Determine the effect of temp & humidity on the device under bias.	JESD22-A110 - 96 hr 130°C - 85% RH Non-Condensing	3 Lot 77 (1)
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	3 Lots 77 (1)
Mechanical	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	2 Lots 77 (1)
	2. Physical Dimensions		JESD22-B100-A	3 Lot 15 (0)
	3. Lead Integrity		EIA/JESD22-B105 Cond. A & B (25 leads/Cond)	N/A for QFP Packages
	4. Solderability		EIA/JESD22-B102 (25 leads)	3 Lot 25(1)
	5. Mark Permanency		EIA/JESD22-B107	3 Lot 25 (1)
ESD	1. HBM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	HBM per EIA/JESD22-A114	2 Lot 3
	2. CDM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	CDM per JESD22-C101	2 Lot 3

Note: Autoclave, HAST & Temperature Cycle groups received preconditioning.

Summary of Results:

Table 3 lists the status and results of the qualification testing for the 100mm TQHIF qualification.

(The results of the tests are summarized in the following section.)

Table 3. Qualification Test Results Summary.

Test Description	Sample Size	Status	Results Lot 1	Results Lot 2	Results Lot 3
◆ Wafer Level Qualification					
Un-Bias Bake	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Temperature Cycle	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Autoclave	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
◆ Qualification Vehicle - TQ7132					
Bias Life test	2 Lots each 77 (1)	Complete	77(0)	77(0)	
PreConditioning (Level 1)	2 Lots each 160 (1)	Complete	239(1)	240(0)	
Autoclave	2 Lots each 77 (1)	Complete	76(1)	77(0)	
HAST	2 Lots each 77 (1)	Complete	77(0)	77(0)	
Temperature Cycle	2 Lots each 77 (1)	Complete	77(0)	76(1)	
Thermal Shock	2 Lots each 77 (1)	Complete	77(0)	77(0)	
Mechanical Analysis	2 Lots	Complete	Passed		
ESD Sensitivity HBM	1 Lot 3	Complete	Passed 750V		
ESD Sensitivity CDM	1 Lot 3	Complete	Passed 1,500		
◆ Qualification Vehicle - TQ7125					
Bias Life test	1 Lot each 77 (1)	Complete	76(0)		
PreConditioning (Level 1)	1 Lot each 160 (1)	Complete	240(0)		
Autoclave	1 Lot each 77 (1)	Complete	77(0)		
HAST	1 Lot each 77 (1)	Complete	77(0)		
Temperature Cycle	1 Lot each 77 (1)	Complete	77(0)		
Thermal Shock	1 Lot each 77 (1)	Complete	77(0)		
Mechanical Analysis	1 Lot	Complete	Passed		
ESD Sensitivity HBM	1 Lot 3	Complete	Passed 500V		
ESD Sensitivity CDM	1 Lot 3	Complete	Passed 3,000V		

Test Results - Wafer Level Qualification:**Unbiased High Temperature Wafer Bake**

Procedure: The wafers are baked at 275°C in air for 168 hours with interim data taken at 0, 96 and 168 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: High temperature bake is performed in air for acceleration of thermally activated failure mechanisms. A temperature of 275°C provides for maximum acceleration without compromising the dielectric material. This test is designed to simulate >20 years of life at 150°C.

Results: Based on analysis, the results on all three wafer lots was acceptable.

Unbiased Autoclave.

Procedure: The wafers are stressed for 96 hours at 121°C, 100% relative humidity at two atmospheres of pressure with interim data taken at 0, 48 and 96 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture into the wafer.

Results: Based on analysis, the results on all three wafer lots was acceptable.

Thermal cycling.

Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 500 cycles with interim data taken at 0, 250 and 500 cycles. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to determine the resistance of a wafer to alternating extremes of high and low temperatures.

Results: Based on analysis, the results on all three wafer lots was acceptable.

Test Results - Product Level Qualification:

HTOL (High Temperature Operating Lifetest)

TQS Test# 1723, 1802, 1862

- Procedure: In general, the life test procedure follows MIL-STD-883, Method 1005, Condition B or JESD22-A108.
- Purpose: Lifetesting is performed for the purpose of demonstrating that device failure rates do not exceed 100 FIT (FIT = Failure unit = failures per billion device hours) for the first 20 years of life at the specified maximum rated operating temperature.
- Results: Vehicle #1 TQ7132
 Test# 1723 - 77 parts from lot B043 were subjected to 1,000 hr. of HTOL.
 - All 77 parts passed electrical test.
 Test# 1802 - 77 parts from lot B356 were subjected to 1,000 hr. of HTOL.
 - All 77 parts passed electrical test.
 Vehicle #2 TQ7125
 Test# 1862 - 77 parts from lot B272 were subjected to 1,000 hr of HTOL.
 - 76 parts passed electrical test, one (1) part was damaged in the handler.

◆ Environmental Test Group

Preconditioning

TQS Test# 1722, 1801, 1861

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
 (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
 (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results: Vehicle #1 TQ7132
 Test# 1722 - 240 parts from lot B043 were subjected to level 1 preconditioning
 - 239 parts passed electrical test. One part failed due to a shorted capacitor.
 Test# 1801 - 240 parts from lot B356 were subjected to level 1 preconditioning
 - All parts passed electrical test.
 Vehicle #2 TQ7125
 Test# 1861 - 240 parts from lot 5655 were subjected to level 1 preconditioning
 - All parts passed electrical test.

Autoclave

TQS Test# 1722, 1801, 1861

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results: Results: Vehicle #1 TQ7132
 Test# 1722 - 77 parts from lot B043 were subjected to 96 hr. of Autoclave
 - 76 parts passed electrical test. One part failed and was destroyed during analysis.
 Test# 1801 - 77 parts from lot B356 were subjected to 96 hr. of Autoclave
 - All passed electrical test.
- Vehicle #2 TQ7125
 Test# 1862 - 77 parts from lot 5655 were subjected to 96 hr. of Autoclave
 - All passed electrical test.

HAST (Highly Accelerated Temperature & Humidity Stress Test)

TQS Test# 1722, 1801, 1861

- Procedure: HAST is performed according to JESD22-A110; with the parts biased and an environment of 131°C 85% RH for 96 hrs.
- Purpose: The purpose of the test is to evaluate the reliability of non-hermetic packaged solid state devices in a biased humid environment. This test usually activates the same type of failures as does biased 85/85 but accelerated by temperature, pressure and humidity.
- Results: Results: Vehicle #1 TQ7132
 Test# 1722 - 77 parts from lot B153 were subjected to 96 hr. of HAST
 - All passed electrical test.
 Test# 1801 - 77 parts from lot B214 were subjected to 96 hr. of HAST
 - All passed electrical test.
- Vehicle #2 TQ7125
 Test# 1861 - 77 parts from lot 5655 were subjected to 96 hr. of HAST
 - All passed electrical test.

Temperature Cycle

TQS Test# 1722, 1801, 1861

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results: Results: Vehicle #1 TQ7132
 Test # 1722 - 77 parts from lot B043 were subjected to 1,000 temperature cycles
 - All parts passed electrical tests.
 Test # 1801 - 77 parts from lot B356 were subjected to 1,000 temperature cycles
 - 76 parts passed electrical tests.
 One (1) part failed due to an open minimum VIA.
- Vehicle #2 TQ7125
 Test # 1861 - 77 parts from lot 5655 were subjected to 1,000 temperature cycles
 - All parts passed electrical tests

◆ Mechanical Test Group

Thermal Shock (Liquid to Liquid)

TQS Test# 1724, 1803, 1863

- Procedure: Thermal Shock is performed according to JESD22-A106 Condition C except -40°C to $+125^{\circ}\text{C}$
- Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.
- Results: Results: Vehicle #1 TQ7132
 Test# 1724 - 77 parts from lot B043 were subjected to 100 thermal shock cycles
 All parts passed electrical test.
 Test# 1803 - 77 parts from lot B356 were subjected to 100 thermal shock cycles
 All parts passed electrical test.
- Vehicle #2 TQ7125
 Test# 1863 - 77 parts from lot 5655 were subjected to 100 thermal shock cycles
 All parts passed electrical test.

Physical Dimensions

TQS Test# 1724, 1803, 1863

- Procedure: The test shall be performed according to JESD22-B100.
- Purpose: The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable documents.
- Results: Vehicle #1 TQ7132 - (4X4-16 MLF)
 Test#1724 - 15 parts from lot B043 were subjected to Physical Dimension verification with no failures.
 Test#1803 - 15 parts from lot B356 were subjected to Physical Dimension verification with no failures.
- Vehicle #2 TQ7125 - (3X3-16 MLF)
 Test#1863 - 15 parts from lot 5655 were subjected to Physical Dimension verification with no failures.

Lead Integrity

- Procedure: The test shall be performed according to JESD22-B105 Cond. A & B.
- Purpose: The purpose of the test is to determine the integrity of the lead/package interface and the lead itself where the lead(s) are bent due to faulty board assembly followed by rework of the parts for re-assembly
- Results: This test is not applicable for leadless packages such as the MLP package

Marking Permanency

TQS Test# 1724, 1803, 1863

Procedure: The test shall be performed according to JESD22-B107.

Purpose: The purpose of the test is to verify that the markings on the device will not become illegible when subjected to solvents of cleaning solutions commonly used during the removal of solder flux residue from the board assembly process

Vehicle #1 TQ7125 - (3X3-16 MLF)

Test# 1724 - 25 parts from lot B043 were subjected to marking permanency testing with no failures.

Test# 1803 - 25 parts from lot B356 were subjected to marking permanency testing with no failures.

Vehicle #2 TQ7125 - (3X3-16 MLF)

Test# 1863 - 25 parts from lot 5655 were subjected to marking permanency testing with no failures.

Solderability

TQS Test# 1724, 1803, 1863

Procedure: The test shall be performed according to JESD22-B102.

Purpose: The purpose of this test is to provide a means of determining the solderability of devices package termination's that are intended to be joined to another surface using solder for the attachment.

Vehicle #1 TQ7125 - (3X3-16 MLF)

Test# 1724 - 25 leads (5 parts) from lot B043 were subjected to solderability testing with no failures.

Test# 1803 - 25 leads (5 parts) from lot B356 were subjected to solderability testing with no failures.

Vehicle #2 TQ7125 - (3X3-16 MLF)

Test# 1863 - 25 leads (5 parts) from lot 5655 were subjected to solderability testing with no failures.

◆ ESD Test Group

ESD Testing (HBM)

TQS Test# 1792, 1774

Procedure: HBM ESD testing is performed per EIA/JESD22-A114

Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic HBM discharge.

Results: Vehicle #1 TQ7132
 Test# 1792 - 3 parts from lot B043 were subjected to HBM ESD stress at 750V with no electrical failures.

Vehicle #2 TQ7125
 Test# 1774 - 3 parts from lot 5002 were subjected to HBM ESD stress at 500V with no electrical failures.

ESD Testing (CDM)

TQS Test# 1793, 1687

Procedure: CDM ESD testing is performed per EIA/JESD22-C101

Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic CDM discharge.

Results: Results: Vehicle #1 TQ7132
 Test# 1793 - 3 parts from lot B043 were subjected to CDM ESD stress at 1,500V with no electrical failures.

Vehicle #2 TQ7125
 Test# 1687 - 3 parts from lot 5002 were subjected to CDM ESD stress at 3,000V with no electrical failures.

□ Conclusion

The 100mm HBT process has successfully completed wafer level PCM reliability testing and product level reliability testing as described in this report and is considered qualified.