

## Process Qualification

*Qualification of the 150 MM - TQRLC Process*

### Abstract

This report summarizes the reliability testing that has been completed to qualify TriQuint's 150MM TQRLC passive process.

### Wafer Level Reliability Testing:

The primary vehicle for wafer-level reliability evaluation is a specifically designed reliability process control monitor. This mask set contains structures intended to address known reliability concerns. The reliability mask set consists of various structures designed to evaluate the reliability of the different passive components that can be manufactured on the TQRLC process.

### Product Level Reliability Testing:

The product test vehicle selected for this qualification.

TQ-1303 - A "0-Degree" Passive Power Divider

The TQ-1303 is fabricated on TriQuint's TQRLC Process and is packaged in a 2X2 MLG5/LPCC5 package. Assembly and encapsulation of the test samples were accomplished at supplier C. Tests, test sample size and failure criteria were defined from TriQuint's Specification REL.021 (Policy and Procedure for Reliability Qualifications of ICs). Most tests outlined in this procedure follow the JEDEC Standard Number 26-A or MIL-STD-883 when applicable.

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## Process Description

TriQuint's TQRLC is a low-cost, pure passives process. This process, fabricated at TriQuint's Hillsboro, Oregon facility, targets the high-performance, small-size passives-only circuits and utilizes over 9 um of gold metal. High-density interconnections are accomplished with three thick global and one surface metal interconnect layers. The four metal layers are encapsulated in a high-performance, low-dielectric constant material that allows wiring flexibility and plastic package simplicity. Precision thin-film NiCr resistors, high-Q inductors (> 50 @ 2 GHz), and high-value MIM capacitors are available.

## Wafer Level Reliability Testing:

The primary vehicle for wafer-level reliability evaluation is a specifically designed reliability process control monitor. This vehicle contains structures intended to address known interconnect reliability issues based on data from the TQTRx process. The reliability process control monitor consists of various structures designed to evaluate the robustness of the different passive components that can be manufactured on the TQRLC process. These structures include thin-film NiCr resistors, large-area MIM capacitors, via contact chains with various sizes and density of metal links, metal leakage combs with various spacings/gaps, and other proprietary structures. In addition, general robustness and capabilities of the process to produce circuit elements can be assessed using this vehicle.

## Product Level Reliability Testing

### Product Description

The TQ1303 is a passive power splitter. This device is used to split one power input into two power outputs, with minimal degradation. The input and outputs are matched to 50 ohms and by keeping the 100 ohm resistor off-chip it allows for high power capacity. The splitter operates at  $741 \pm 19$  MHz and performs power splitting functions typically found in the VCO chain of Cellular handsets

**Test Plan:**

Table 1 & 2 list the qualification plan for TQRLC. This plan is based on the requirements of REL.021

**Table 1. Wafer Level Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
<b>Environmental</b>	1. High Temperature Unbiased Bake	Determine the effect of High Temperature Storage.	275°C Air Bake 168 hrs	3 Lots 1 Wafer/Lot
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 1 Wafer/Lot
	3. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 500 Cycles	3 Lots 1 Wafer/Lot

**Table 2. Device Qualification Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
<b>MSL</b>	1. Moisture Sensitivity Level Testing		IPC/JESD J-STD-020 Moisture/Reflow Sensitivity Classification of Non-Hermetic Solid State Surface Mount Devices	1 Lot
<b>HTOL</b>	1. High Temperature Storage	Determine the effect of temp on the device over an extended period of time	JESD22-A103-A Ambient = 150°C 1000 Hours Minimum	3Lot 77 (1)
<b>Environmental</b>	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	3 Lot 320 (1)
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lot 77 (1)
	3. HAST	Determine the effect of temp & humidity on the device under bias.	JESD22-A110 - 96 hr 130°C - 85% RH Non-Condensing	3 Lot 77 (1)
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	3 Lot 77 (1)
<b>Mechanical</b>	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	3 Lot 77 (1)
	2. Physical Dimensions		JESD22-B100-A	2 Lot 15 (0)
	3. Lead Integrity		EIA/JESD22-B105 Cond. A & B (25 leads/Cond)	N/A for MLF
	4. Mark Permanency		EIA/JESD22-B107	3 Lot 25 (1)
	5. Solderability		EIA/JESD22-B102 Cond A	2 Lot 5(0)
<b>ESD</b>	1. ESD Sensitivity	Determine the sensitivity of the device to levels of ESD	HBM per EIA/JESD22-A114	1 Lot 3
	2. ESD Sensitivity		CDM per JESD22-C101	1 Lot 3

Note: HAST, Autoclave, & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

## Summary of Results:

Table 3 lists the status and results of the qualification testing for TQRLC.

**Table 3. Qualification Test Results Summary.**

Test Description	Sample Size	Status	Results Lot 1	Results Lot 2	Results Lot 3
<b>◆ Wafer Level Qualification</b>					
Un-Bias Bake	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Temperature Cycle	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Autoclave	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
<b>◆ Qualification Vehicle</b>					
High Temperature Storage	3Lot 77 (1)	Complete	76(0)	77(0)	77(0)
PreConditioning	3 Lot 240 (1)	Complete	240(0)	240(0)	240(0)
Autoclave	3 Lot 77 (1)	Complete	77(0)	76(0)	77(0)
HAST	3 Lot 77 (1)	Complete	77(0)	77(0)	77(0)
Temperature Cycle	3 Lot 77 (1)	Complete	76(1)	77(0)	77(0)
Thermal Shock	3 Lot 77 (1)	Complete	77(0)	77(0)	75(0)
Physical Dimensions	2 Lot 15 (0)	Complete	Passed	Passed	Passed
Lead Integrity	N/A				
Mark Permanency	2 Lot 25 (1)	Complete	Passed	Passed	Passed
Solderability	2 Lot 5(0)	Complete	Passed	Passed	Passed
ESD Sensitivity HBM	1 Lot 3	Complete	Passed 350V		
ESD Sensitivity CDM	1 Lot 3	Complete	Passed 3,000V		

## **Test Results - Wafer Level Qualification:**

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### **Unbiased High Temperature Wafer Bake**

- Procedure: The wafers are baked at 275°C in air for 168 hours with data taken at 0 and 168 hours. Testing is done on one (1) wafer minimum (typically 55 tiles per wafer) per lot.
- Purpose: High temperature bake is performed in air for acceleration of thermally activated failure mechanisms. A temperature of 275°C provides for maximum acceleration without compromising the dielectric material. This test is designed to simulate >20 years of life at 150°C.
- Results: Based on the analysis done on Lot#s A121504B, A123302A, A125704A & A129803A, the results on all four wafer lots was acceptable.

### **Unbiased Autoclave.**

- Procedure: The wafers are stressed for 96 hours at 121°C, 100% relative humidity at two atmospheres of pressure with data taken at 0 and 96 hours. Testing is done on one (1) wafer minimum (typically 55 tiles per wafer) per lot.
- Purpose: The purpose of this test is to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture into the wafer.
- Results: Based on the analysis done on Lot#s A121504B, A123302A, A125704A & A129803A, the results on all four wafer lots was acceptable.

### **Thermal cycling.**

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 500 cycles with data taken at 0 and 500 cycles. Testing is done on one (1) wafer minimum (typically 55 tiles per wafer) per lot.
- Purpose: The purpose of this test is to determine the resistance of a wafer to alternating extremes of high and low temperatures.
- Results: Based on the analysis done on Lot#s A121504B, A123302A, A125704A & A129803A, the results on all four wafer lots was acceptable.

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## Test Status:

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### High Temperature Storage

TQS Test#1772, 1839 & 1842

- Procedure: In general, the life test procedure follows IPC/JESD22-020.
- Purpose: Determine the effect of High Temperature Storage on the life of a device over an extended period of time.
- Results:
- Test# 1772 - 76 parts from lot B184 passed electrical test after 1,000 hrs of Bake  
One (1) part was damaged in the handler
  - Test# 1839 - 77 parts from lot B470 passed electrical test after 1,000 hrs of Bake
  - Test# 1842 - 77 parts from lot B466 passed electrical test after 1,000 hrs of Bake

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## ◆ Environmental Test Group

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### Preconditioning

TQS Test#1756, 1773 & 1840

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
- (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
  - (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results:
- Test# 1756 - 240 parts from lot B184 passed electrical test after preconditioning
  - Test# 1773 - 240 parts from lot B470 passed electrical test after preconditioning
  - Test# 1840 - 240 parts from lot B466 passed electrical test after preconditioning

### Autoclave

TQS Test#1756, 1773 & 1840

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results:
- Test# 1756 - 77 parts from lot B184 passed electrical test after 96 hrs of Autoclave
  - Test# 1773 - 76 parts from lot B470 passed electrical test after 96 hrs of Autoclave  
One (1) part was damaged in the handler.
  - Test# 1840 - 77 parts from lot B466 passed electrical test after 96 hrs of Autoclave

### HAST (Highly Accelerated Temperature & Humidity Stress Test)

TQS Test#1756, 1773 & 1840

- Procedure: HAST is performed according to JESD22-A110; with the parts biased and an environment of 131°C 85% RH for 96 hrs.
- Purpose: The purpose of the test is to evaluate the reliability of non-hermetic packaged solid state devices in a biased humid environment. This test usually activates the same type of failures as does biased 85/85 but accelerated by temperature, pressure and humidity.
- Results:
- Test# 1756 - 77 parts from lot B184 passed electrical test after 96 hrs of Biased HAST.
  - Test# 1773 - 77 parts from lot B470 passed electrical test after 96 hrs of Biased HAST.
  - Test# 1840 - 77 parts from lot B466 passed electrical test after 96 hrs of Biased HAST.

**Temperature Cycle**

TQS Test#1756, 1773 & 1840

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results: - Test# 1756 - 76 parts from lot B184 passed electrical test after 1,000 Temp Cycles.  
One (1) part failed for Ball Bond Lift  
- Test# 1773 - 76 parts from lot B470 passed electrical test after 1,000 Temp Cycles.  
One (1) part was damaged in the handler  
- Test# 1840 - 77 parts from lot B466 passed electrical test after 1,000 Temp Cycles.

**◆ Mechanical Test Group**

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**Thermal Shock (Liquid to Liquid)**

TQS Test# 1788, 1841 & 1844

- Procedure: The test shall be performed according to JESD22-A106 Condition C except -40°C to +125°C
- Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.
- Results: - Test# 1788 - 77 parts from lot B184 passed electrical test after 100 Temp Shock Cycles.  
- Test# 1841 - 77 parts from lot B470 passed electrical test after 100 Temp Shock Cycles.  
- Test# 1844 - 75 parts from lot B466 passed electrical test after 100 Temp Shock Cycles.  
Two (2) parts were damaged in the handler.

**Physical Dimensions**

TQS Test# 1788, 1841 & 1844

- Procedure: The test shall be performed according to JESD22-B100.
- Purpose: The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable documents.
- Results: - Test# 1788 - 15 parts from lot B184 met all dimensional criteria.  
- Test# 1841 - 15 parts from lot B470 met all dimensional criteria.  
- Test# 1844 - 15 parts from lot B466 met all dimensional criteria.

**Lead Integrity**

TQS Test# N/A

- Procedure: The test shall be performed according to JESD22-B105 Cond. A & B.
- Purpose: The purpose of the test is to determine the integrity of the lead/package interface and the lead itself where the lead(s) are bent due to faulty board assembly followed by rework of the parts for re-assembly
- Results: - Not Applicable

**Marking Permanency**

TQS Test# 1788, 1841 & 1844

- Procedure: The test shall be performed according to JESD22-B107.
- Purpose: The purpose of the test is to verify that the markings on the device will not become illegible when subjected to solvents of cleaning solutions commonly used during the removal of solder flux residue from the board assembly process
- Results: - Test# 1788 - 25 parts from lot B184 passed the marking permanency test.  
- Test# 1841 - 15 parts from lot B470 passed the marking permanency test.  
- Test# 1844 - 15 parts from lot B466 passed the marking permanency test.

**Solderability**

TQS Test# 1788, 1841 & 1844

- Procedure: The test shall be performed according to JESD22-B102.
- Purpose: The purpose of this test is to provide a means of determining the solderability of devices package terminations that are intended to be joined to another surface using solder for the attachment.
- Results: - Test# 1788 - 5 parts from lot B184 passed the solderability testing.  
- Test# 1841 - 5 parts from lot B470 passed the solderability testing.  
- Test# 1844 - 5 parts from lot B466 passed the solderability testing.

**◆ ESD Test Group**

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**ESD Testing (HBM)**

TQS Test#1543

- Procedure: This testing will be performed per EIA/JESD22-A114
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic HBM discharge.
- Results: Three parts from lot#: B184 were subjected to 350V stress with no failures at electrical test

**ESD Testing (CDM)**

TQS Test# 1543

- Procedure: This testing will be performed per EIA/JESD22-C101
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic CDM discharge.
- Results: Three parts from lot#: B184 were subjected to 3,000V stress with no failures at electrical test

**□ Conclusion**

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The 150mm TQRLC process has successfully completed all reliability testing per the requirements specified in REL.021 and is considered qualified.