

Qualification Report

Qualification of the 150mm QEDA2 Process

Abstract

This report summarizes the reliability tests that were completed to qualify TriQuint Semiconductor's conversion of its QEDA2 0.6 μ m E/D MESFET GaAs wafer fabrication process from 100mm wafers to 150mm wafers.

Wafer Level Reliability Testing:

A reliability mask set specifically designed to address the concerns identified during a Failure Modes and Effects Analysis (FMEA).

Product Level Reliability Testing:

Test Vehicle #1: A 4X4 Cross Point which is fabricated on TriQuint's QEDA2 0.6 μ m E/D MESFET GaAs process and is packaged in a TSSOP28 package. Assembly and encapsulation of the test samples were accomplished at supplier A.

Test Vehicle #2: A Demultiplexer which is fabricated on TriQuint's QEDA2 0.6 μ m E/D MESFET GaAs process and is packaged in a 208 BGA package. Assembly and encapsulation of the test samples were accomplished at supplier A.

Tests, test sample size and failure criteria were defined from TriQuint's Specification REL.021 (Policy and Procedure for Reliability Qualifications of ICs). Most tests outlined in this procedure follow the JEDEC Standard Number 26-A or MIL-STD-883 when applicable.

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Process Description

TriQuint's QEDA2 process is a Gallium Arsenide (GaAs) semiconductor process fabricated at TriQuint's Hillsboro, Oregon facility

This process was originally qualified on 100mm wafers in 1998

- ◆ Photolithography Layers = 17
- ◆ Global metallization Layers = 3
- ◆ Plated Gold Interconnects
- ◆ Low TCR Nichrome Resistors
- ◆ Gate Length = 0.6 μ m
- ◆ Gate Ti Thickness = 500A
- ◆ Low K Planarizing Interlayer Dielectric
- ◆ Etc

Wafer Level Reliability Testing

The primary vehicle for wafer-level reliability evaluation is a specifically designed reliability mask set. This mask set contains structures intended to address the concerns identified during a Failure Modes and Effects Analysis (FMEA). The reliability mask set consists of various structures designed to evaluate the reliability of the different passive and active components that can be manufactured on the QEDA2 process. These structures include individual active devices, large capacitors, various via and contact chains, long interconnect meanders, wide area leakage combs, and several specific proprietary structures for highly accelerated on-wafer reliability assessment. In addition, general robustness and capabilities of the process to produce circuit elements can be assessed using this vehicle.

Product Level Reliability Testing

Qualification Vehicle

The 4x4 digital crosspoint is a non-blocking switch capable of data rates up to 2.7Gb/s gigabits per second per port. Utilizing a fully differential internal data path and LVPECL I/O with on-chip 50 Ω terminations, the crosspoint offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise-rejection characteristics inherent in differential logic result in low jitter and signal skew.

The demultiplexer is a multi-configuration SONET/SDH OC48/STM16 CDR/DEMUX that regenerates and re-times serial 2.48832 Gb/s data. It recovers the 2.48832 GHz clock from the data stream and frequency divides it to generate control signals and clocks used to perform the demultiplexing function.

Test Plan:**Table 1. Wafer Level Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
Environmental	1. High Temperature Unbiased Bake	Determine the effect of High Temperature Storage.	275°C Air Bake 168 hrs	3 Lots 1 Wafer/Lot
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 1 Wafer/Lot
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 500 Cycles	3 Lots 1 Wafer/Lot

Table 2. Product Level Qualification Test Plan.

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
HTOL	1. Biased Life test	Determine the effect of bias and temp on the device over an extended period of time.	VDD biased at 2.8 V 1,000 hrs Ambient Temperature, 125°C	3 Lots 77 (1)
Environmental	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	3 Lots 240 (1)
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 77 (1)
	3. HAST	Determine the effect of temp & humidity on the device under bias.	JESD22-A110 - 96 hr 130°C - 85% RH Non-Condensing	3 Lots 77 (1)
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	3 Lots 77 (1)
Mechanical	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	3 Lots 77 (1)
ESD	1. ESD Sensitivity HBM	Determine the sensitivity of the device to levels of ESD.	HBM per EIA/JESD22-A114	1 Lots 3
	2. ESD Sensitivity CDM		CDM per EIA/JESD22-C101	1 Lots 3

Note: HAST, Autoclave, & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

Summary of Results:

Table 3 lists the results of the qualification testing for the 150mm qualification.

(The detail test results is listed in the following section.)

Table 3. Qualification Test Results Summary.

Test Description	Sample Size	Status	Results Lot 1	Results Lot 2	Results Lot 3
◆ Wafer Level Qualification					
Unbiased Bake	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Autoclave	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
Temperature Cycle	3 Lots 1 Wafer/Lot	Complete	Passed	Passed	Passed
◆ Product Qualification - Test Vehicle #1 - 4X4 Crosspoint					
Bias Life test	3 Lots each 77 (1)	Complete	77(0)	77(0)	77(0)
PreConditioning	3 Lots each 240 (1)	Complete	240(0)	240(0)	240(0)
Autoclave	3 Lots each 77 (1)	Complete	77(0)	77(0)	77(0)
Temperature Cycle	3 Lots each 77 (1)	Complete	77(0)	77(0)	77(0)
Thermal Shock	3 Lots each 77 (1)	Complete	77(0)	77(0)	77(0)
ESD Sensitivity HBM/CDM	1 Lots 3	Complete	HBM >2,000V CDM > 1,500V		
◆ Product Qualification - Test Vehicle #2 - DeMux					
Bias Life test	2 Lots each 45 (0)	Complete	45(0)	45(0)	
PreConditioning	Not Required				
Autoclave	2 Lots each 45 (0)	Complete	45(0)	45(0)	
Temperature Cycle	2 Lots each 45 (0)	Complete	45(0)	45(0)	
Thermal Shock	2 Lots each 45 (0)	Complete	45(0)	45(0)	

Test Results - Wafer Level Qualification:

Unbiased High Temperature Wafer Bake

Procedure: The wafers are baked at 275°C in air for 168 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: High temperature bake is performed in air for acceleration of thermally activated failure mechanisms. A temperature of 275°C provides for maximum acceleration without compromising the dielectric material. This test is designed to simulate >20 years of life at 150°C.

Results: One (1) wafer from each of three (3) Lots (A1110701A, A114002A & A114803A) fabricated using reliability mask set 4576, was subjected to a 275 °C bake for 168 hrs. The following features on the mask were tested after stress: Via Structures, Capacitors, FETS, Diodes, Ohmic TLMs, NiCr Resistors, Combs Structures and Meander Lines.

All structures, on all three (3) wafers tested were acceptable.

Unbiased Autoclave.

Procedure: The wafers are stressed for 96 hours at 121°C, 100% relative humidity at two atmospheres of pressure with interim data taken at 0, 48 and 96 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture into the wafer.

Results: One (1) wafer from each of three (3) Lots (A1110701A, A114002A & A114803A) fabricated using reliability mask set 4576, was subjected to 96 hrs of autoclave. The following features on the mask were tested after stress: Via Structures, Capacitors, FETS, Diodes, Ohmic TLMs, NiCr Resistors, Combs Structures and Meander Lines.

All structures, on all three (3) wafers tested were acceptable.

Thermal cycling.

Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 500 cycles with interim data taken at 0, 250 and 500 cycles. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to determine the resistance of a wafer to alternating extremes of high and low temperatures.

Results: One (1) wafer from each of three (3) Lots (A1110701A, A114002A & A114803A) fabricated using reliability mask set 4576, was subjected to 500 temperature cycles between -40°C to +125°C. The following features on the mask were tested after stress: Via Structures, Capacitors, FETS, Diodes, Ohmic TLMs, NiCr Resistors, Combs Structures and Meander Lines.

All structures, on all three (3) wafers tested were acceptable.

Test Results - Product Level Qualification:

HTOL (High Temperature Operating Lifetest)

TQS Test#1322, 1323, 1619, 1629 & 1632

- Procedure: In general, the life test procedure follows MIL-STD-883, Method 1005, Condition B or JESD22-A108.
- Purpose: Lifetesting is performed for the purpose of demonstrating that device failure rates do not exceed 100 FIT (FIT = Failure unit = failures per billion device hours) for the first 20 years of life at the specified maximum rated operating temperature.
- Results: Test Vehicle #1
 Test# 1322 - 77 parts from lot 4079 were subjected to 1,000 of HTOL.
 - All passed electrical test
 Test# 1323 - 77 parts from lot 4560 were subjected to 1,000 of HTOL.
 - All passed electrical test
 Test# 1619 - 77 parts from lot 4561 were subjected to 1,000 of HTOL.
 - All passed electrical test
Test Vehicle #2
 Test# 1629 - 45 parts from lot 4529 were subjected to 1,000 of HTOL.
 - All passed electrical test
 Test# 1632 - 45 parts from lot 4522 were subjected to 1,000 of HTOL.
 - All passed electrical test

◆ Environmental Test Group

Preconditioning

TQS Test# 1318, 1321, 1618, 1634 & 1630

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
- (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
 - (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results: Test Vehicle #1
 Test# 1318 - 240 parts from lot 4079 were subjected to level 1 preconditioning
 - All passed electrical test.
 Test# 1321 - 240 parts from lot 4560 were subjected to level 1 preconditioning
 - All passed electrical test.
 Test# 1618 - 240 parts from lot 4561 were subjected to level 1 preconditioning
 - All passed electrical test.
Test Vehicle #2
 Test# 1634 - Preconditioning Not Required
 Test# 1630 - Preconditioning Not Required

Autoclave

TQS Test# 1318, 1321, 1618, 1634 & 1630

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results: Test Vehicle #1
 Test# 1318 - 77 parts from lot 4079 were subjected to 96 hr. of Autoclave
 - All passed electrical test.
 Test# 121 - 77 parts from lot 4560 were subjected to 96 hr. of Autoclave
 - All passed electrical test.
 Test# 1618 - 77 parts from lot 4561 were subjected to 96 hr. of Autoclave
 - All passed electrical test.
Test Vehicle #2
 Test# 1634 - 45 parts from lot 4529 were subjected to 96 hr. of Autoclave
 - All passed electrical test.
 Test# 1630 - 45 parts from lot 4522 were subjected to 96 hr. of Autoclave
 - All passed electrical test.

Temperature Cycle

TQS Test# 1318, 1321, 1618, 1634 & 1630

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results: Test Vehicle #1
 Test # 1318 - 77 parts from lot 4079 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.
 Test # 1321 - 77 parts from lot 4560 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.
 Test # 1618 - 77 parts from lot 4561 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.
Test Vehicle #2
 Test # 1634 - 45 parts from lot 4529 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.
 Test # 1630 - 45 parts from lot 4522 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.

◆ Mechanical Test Group

Thermal Shock (Liquid to Liquid)

TQS Test# 1324, 1325, 1620, 1631 & 1636

Procedure: The test shall be performed according to JESD22-A106 Condition C except -40°C to +125°C.

Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.

Results: Test Vehicle #1

Test# 1324 - 77 parts from lot 4079 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

Test# 1325 - 77 parts from lot 4560 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

Test# 1620 - 77 parts from lot 4561 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

Test Vehicle #2

Test# 1631 - 45 parts from lot 4529 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

Test# 1636 - 45 parts from lot 4522 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

◆ ESD Test Group

ESD Testing (HBM)

TQS Test# 1320

Procedure: HBM ESD testing is performed per EIA/JESD22-A114

Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic HBM discharge.

Results: Test#1320 - All parts from lot 4079 passed electrical test after being exposed to 2,000 volts.

ESD Testing (CDM)

TQS Test# 1319

Procedure: CDM ESD testing is performed per EIA/JESD22-C101

Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic CDM discharge.

Results: Test#1319 - All parts from lot 4079 passed electrical test after being exposed to 1,500 volts.

□ Conclusion

The 150mm QEDA2 process has successfully completed all reliability testing per the requirements specified in REL.021 and is considered qualified.