

# Process Qualification

## *Qualification of the TQHIF Process*

### **Abstract**

This report summarizes the reliability tests performed to qualify TriQuint Semiconductor's TQHIF GaAs wafer fabrication process on 100mm Wafers.

### **Wafer Level Reliability Testing:**

On-wafer process control monitor (PCM) structures representative of circuit elements.

### **Product Level Reliability Testing:**

Two representative product test vehicles were selected for this qualification.

**Qualification Vehicle "A" - TQ-8218 - Laser Driver.**

**Qualification Vehicle "B" - TQ-8726 - Demultiplexer .**

*( Both products are packaged in a qualified TSSOP-28 package from qualified subcontractor A1. )*

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## Process Description

TriQuint's TQHIF is an advanced Gallium Arsenide (GaAs) 0.3 micron enhancement/depletion mode MESFET process with one level of local interconnects and three levels of electroplated Au global metal interconnects. The process has been optimized for the combination of high speed ( $f_t > 50\text{GHz}$ ), high breakdown ( $BV > 10\text{V}$ ), and high gain (reduced short-channel effects and high  $G_m$ ). The process uses ion-implantation technology to enable both E-mode ( $V_p = 0\text{mV}$ ) and D-mode ( $V_p = -500\text{mV}$ ) MESFETs, half-FET Schottky diodes, N+ overlap Schottky diodes, varactors, and on-chip ESD protection. This process is fabricated at TriQuint's Hillsboro, Oregon facility. It supports digital and mixed signal applications for 2.7 Gb/s (OC-48) and 10.7 Gb/s (OC-192) telecom and fiber optic markets with supply voltages of 3.3-5.0V. The three global metal layers are encapsulated in a high performance, planarizing, low-k interlayer dielectric that enables wiring flexibility and density, robust inductor and VCO design, and plastic packaging. Precision NiCr resistors, implanted D- resistors, and high value MIM capacitors are included in this process.

## Wafer Level Reliability Testing:

The vehicle for wafer-level reliability evaluation was the on-wafer process control monitor (PCM) structures. The PCM structures are representative of the various passive and active components manufactured with the TQHIF process. These structures include individual active devices, capacitors, various via and contact chains, leakage combs and other proprietary structures.


## Product Level Reliability Testing

### Qualification Vehicle "A"

The TQ8218 is a 3.125 Gb/s low jitter, high performance electro/optical driver intended for interfacing LVPECL outputs from a multiplexer device to various E/O devices, including uncooled DFB lasers, high power VCSEL arrays, EA modulators and Mach-Zehnder modulators. The devices' symmetry and level controls, low additive jitter, and excellent rise/fall times while driving significant loads allow the highest system level performance at low cost.

### Qualification Vehicle "B"

The TQ8726 is a 1:8 Demultiplexer which accepts a differential LVPECL serial NRZ input data signal (DIN, NDIN) and deserializes it into an 8 bit LVDS word (RDO, NRDO - RD7, NRD7). The TQ8726 operates at a serial input data rate of up to 2.7 Gb/s. Timing functions are performed on-chip by a Clock Divide Chain which utilizes an externally AC coupled differential serial input bit clock (RCLK, NRCLK). The external clock allows for arbitrary data rates to be used. The clock divide generates an LVDS parallel byte clock (BCLK, NBCLK). Both the serial clock and data inputs have onchip 50 Ohm terminations and bias circuits, which eases board layout. The DIN termination resistors are connected to VTT, which is brought out to a package pin. This allows the termination voltage to be set for either AC or DC coupled data.

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	<b>Reliability Test Report</b>

11/13/01

**Test Plan:****Table 1. Wafer Level Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
<b>Environmental</b>	1. High Temperature Unbiased Bake	Determine the effect of High Temperature Storage.	275°C Air Bake 168 hrs	3 Lots 1 Wafer/Lot
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 1 Wafer/Lot
	3. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 500 Cycles	3 Lots 1 Wafer/Lot

**Table 2. Product Level Qualification Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
<b>HTOL</b>	1. Bias Life test	Determine the effect of bias and temp on the device over time.	1,000 hrs @ Bias & Ambient Temp. conditions adjusted to raise the Junction Temp. to ~150°C	3 Lots 77 (1)
<b>Environmental</b>	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	3 Lots 160 (1)
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lots 77 (1)
	3. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	3 Lots 77 (1)
<b>Mechanical</b>	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	2 Lots 77 (1)
<b>ESD</b>	1. HBM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	HBM per EIA/JESD22-A114	1 Lot 3
	2. CDM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	CDM per JESD22-C101	1 Lot 3

Note: Autoclave & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

## Summary of Results:

Table 3 lists the status and results of the qualification testing for the 100mm TQHIF qualification.

(The present status of the tests is listed in the following section.)

**Table 3. Qualification Test Results Summary.**

Test Description	Sample Size	Status	Results Lot 1	Results Lot 2	Results Lot 3
<b>◆ Wafer Level Qualification</b>					
Un-Bias Bake	3 Lots 1 Wafer/Lot	Complete	Pass	Pass	Pass
Temperature Cycle	3 Lots 1 Wafer/Lot	Complete	Pass	Pass	Pass
Autoclave	3 Lots 1 Wafer/Lot	Complete	Pass	Pass	Pass
<b>◆ Qualification Vehicle "A" - TQ8218</b>					
Bias Life test	3 Lots each 77 (1)	Complete	73(1)	74(3)	75(2)
PreConditioning ( Level 1 )	3 Lots each 160 (1)	Complete	240(0)	234(1)	160(0)
Autoclave	3 Lots each 77 (1)	Complete	77(0)	77(0)	76(1)
Temperature Cycle	3 Lots each 77 (1)	Complete	77(0)	77(0)	77(0)
Thermal Shock	2 Lots each 77 (1)	Complete	77(0)	77(0)	
ESD Sensitivity HBM	1 Lot 3	Complete	>250V		
ESD Sensitivity CDM	1 Lot 3	Complete	>500V		
<b>◆ Qualification Vehicle "B" - TQ8726</b>					
Bias Life test	3 Lots each 77 (1)	3 Lot In-Process	77(0)	77(0)	76(0)
PreConditioning ( Level 1 )	3 Lot each 160 (1)	3 Lot In-Process	157(0)	160(0)	160(0)
Autoclave	3 Lots each 77 (1)	3 Lot In-Process	77(0)	77(0)	77(0)
Temperature Cycle	3 Lots each 77 (1)	3 Lot In-Process	77(0)	77(0)	77(0)
Thermal Shock	1 Lot each 77 (1)	Complete	76(0)		
ESD Sensitivity HBM	1 Lot 3	Complete	>2,000V		
ESD Sensitivity CDM	1 Lot 3	Complete	>1,500V		

**Test Results - Wafer Level Qualification:****Unbiased High Temperature Wafer Bake**

Procedure: The wafers are baked at 275°C in air for 168 hours with interim data taken at 0, 96 and 168 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: High temperature bake is performed in air for acceleration of thermally activated failure mechanisms. A temperature of 275°C provides for maximum acceleration without compromising the dielectric material. This test is designed to simulate >20 years of life at 150°C.

Results: Based on analysis, the results on all three wafer lots was acceptable.

**Unbiased Autoclave.**

Procedure: The wafers are stressed for 96 hours at 121°C, 100% relative humidity at two atmospheres of pressure with interim data taken at 0, 48 and 96 hours. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to apply severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture into the wafer.

Results: Based on analysis, the results on all three wafer lots was acceptable.

**Thermal cycling.**

Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 500 cycles with interim data taken at 0, 250 and 500 cycles. Testing is done on one (1) wafer minimum (typically 20 to 40 tiles per wafer) per lot.

Purpose: The purpose of this test is to determine the resistance of a wafer to alternating extremes of high and low temperatures.

Results: Based on analysis, the results on all three wafer lots was acceptable.

## Test Results - Product Level Qualification:

### HTOL (High Temperature Operating Lifetest)

TQS Test# 1659, 1117, 1120, 1295, 1296 &amp; 1297

Procedure: In general, the life test procedure follows MIL-STD-883, Method 1005, Condition B or JESD22-A108.

Purpose: Lifetesting is performed for the purpose of demonstrating that device failure rates do not exceed 100 FIT (FIT = Failure unit = failures per billion device hours) for the first 20 years of life at the specified maximum rated operating temperature.

Results: **Qualification Vehicle "A" - TQ8218** ( see comments in the conclusion statement )

Test# 1295 - 77 parts from lot 3995 were subjected to 1,000 of HTOL.

- Three (3) parts were damaged in the handler\* and one (1) failed marginal "VOL"
- The remaining 73 parts passed electrical test.

Test# 1296 - 77 parts from lot 4401 were subjected to 1,000 of HTOL.

- Two (2) parts failed for "Output Mismatch" and One (1) part failed for "Vsymx"
- The remaining 74 parts passed electrical test.

Test# 1297 - 77 parts from lot 4532 were subjected to 1,000 of HTOL.

- One (1) parts failed for "Output Mismatch" and One (1) part failed for "Vsymx"
- The remaining 75 parts passed electrical test.

#### Qualification Vehicle "B" - TQ8726

Test# 1659 - 77 parts from lot 4350 completed 1,000 of HTOL with no electrical failures.

Test# 1117 - 76 parts from lot 4395 completed 1,000 of HTOL with no electrical failures.

- One (1) part was damaged in the handler\*.

Test# 1120 - 76 parts from lot 4402 completed 1,000 of HTOL with no electrical failures.

- One (1) part was damaged in the handler\*.

## ◆ Environmental Test Group

### Preconditioning

TQS Test# 1113, 1116, 1119, 1292, 1293 &amp; 1294

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
- (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
  - (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test# 1292 - 240 parts from lot 3995 were subjected to level 1 preconditioning  
 - All passed electrical test.  
 Test# 1293 - 235 parts from lot 4401 were subjected to level 1 preconditioning  
 - One part failed to for "Vsymx" - the remaining 234 parts passed electrical test.  
 Test# 1294 - 160 parts from lot 4532 were subjected to level 1 preconditioning  
 - All passed electrical test.  
**Qualification Vehicle "B" - TQ8726**  
 Test# 1113 - 160 parts from lot 4350 were subjected to level 1 preconditioning  
 - Three (3) parts were damaged in the handler\* - The remaining 157 passed electrical test.  
 Test# 1116 - 160 parts from lot 4395 were subjected to level 1 preconditioning  
 - All passed electrical test.  
 Test# 1119 - 160 parts from lot 4402 were subjected to level 1 preconditioning  
 - All passed electrical test.

### Autoclave

TQS Test# 1113, 1116, 1119, 1292, 1293 &amp; 1294

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test# 1292 - 77 parts from lot 3995 were subjected to 96 hr. of Autoclave  
 - All passed electrical test.  
 Test# 1293 - 77 parts from lot 4401 were subjected to 96 hr. of Autoclave  
 - All passed electrical test.  
 Test# 1294 - 77 parts from lot 4532 were subjected to 96 hr. of Autoclave  
 - One (1) part failed for "Vsymx" - the remaining 76 parts passed electrical test.  
**Qualification Vehicle "B" - TQ8726**  
 Test# 1113 - 77 parts from lot 4350 were subjected to 96 hr. of Autoclave  
 - All passed electrical test.  
 Test# 1116 - 77 parts from lot 4395 were subjected to 96 hr. of Autoclave  
 - All passed electrical test.  
 Test# 1119 - 77 parts from lot 4402 were subjected to 96 hr. of Autoclave  
 - All passed electrical test.

**Temperature Cycle**

TQS Test# 1113, 1116, 1119, 1292, 1293 &amp; 1294

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test # 1292 - 77 parts from lot 3995 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.  
 Test # 1293 - 77 parts from lot 4401 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.  
 Test # 1294 - 77 parts from lot 4532 were subjected to 1,000 temperature cycles from -40°C to +125°C - All parts passed electrical tests.  
**Qualification Vehicle "B" - TQ8726**  
 Test # 1113 - 77 parts from lot 4350 were subjected to 1,000 temperature cycles from -40°C to +125°C - All passed electrical test.  
 Test # 1116 - 77 parts from lot 4395 were subjected to 1,000 temperature cycles from -40°C to +125°C - All passed electrical test.  
 Test # 1119 - 77 parts from lot 4402 were subjected to 1,000 temperature cycles from -40°C to +125°C - All passed electrical test.

**◆ Mechanical Test Group****Thermal Shock (Liquid to Liquid)**

TQS Test# 1115, 1298 &amp; 1299

- Procedure: Thermal Shock is performed according to JESD22-A106 Condition C except -40°C to +125°C
- Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test# 1298 - 77 parts from lot 3995 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.  
 Test# 1299 - 77 parts from lot 4401 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.  
**Qualification Vehicle "B" - TQ8726**  
 Test# 1115 - 77 parts from lot 4350 were subjected to 100 thermal shock cycles between -40°C to +125°C. One (1) part was damaged in the handler\*  
 The remaining 76 all passed electrical test.

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 ◆ ESD Test Group
 

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**ESD Testing (HBM)**

TQS Test# 1134, 1290

- Procedure: HBM ESD testing is performed per EIA/JESD22-A114
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic HBM discharge.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test#1290 - All parts tested passed electrical test after being exposed to 250 volts.  
**Qualification Vehicle "B" - TQ8726**  
 Test#1134 - All parts tested passed electrical test after being exposed to 2,000 volts.

**ESD Testing (CDM)**

TQS Test# 1135, 1291

- Procedure: CDM ESD testing is performed per EIA/JESD22-C101
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic CDM discharge.
- Results: **Qualification Vehicle "A" - TQ8218**  
 Test#1291 - All parts tested passed electrical test after being exposed to 500 volts.  
**Qualification Vehicle "B" - TQ8726**  
 Test#1135 - All parts tested passed electrical test after being exposed to 1,500 volts.

\* **Note:** "damaged in the handler" = because the test products are passed through the test handler multiple times, both before and after stress, the leads can become damaged to the point where it is impossible for them to make contact to the test socket.

**□ Conclusion**

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The wafer level PCM device testing and representative product testing has been completed for the TQHIF process.

Based on the successful completion of wafer level qualification, and product qualification of the TQ8726, the TQHIF is qualified.

**Description of Issue related to the HTOL testing of the TQ8218**

Analysis of the TQ8218 HTOL failures determined the junction temperature during stress was  $>200^{\circ}\text{C}$ ,  $>50^{\circ}\text{C}$  above the target of  $150^{\circ}\text{C}$ . The TQ8218 circuit design and the HTOL operating temperature contributed to the excessive junction temperature. The TQ8218 qualification will be performed again with changes to the circuit design and a lower HTOL operating temperature. The circuit design changes will also address the TQ8218 ESD results.