

TQTRx process Qualification

Abstract

This report summarizes the reliability testing that has been completed to qualify the TQTRx Process.

The qualification vehicle was a MESFET Power Amplifier fabricated on TriQuint's E/D MESFET GaAs process and packaged in a QSOP16 package with a heat slug. Assembly and encapsulation of the test samples were accomplished at supplier A. Tests, test sample size and failure criteria were defined from TriQuint's Specification REL.021 (Policy and Procedure for Reliability Qualifications of ICs). Most tests outlined in this procedure follow the JEDEC Standard Number 26-A or MIL-STD-883 when applicable.

For further information please contact:

TriQuint Semiconductor

2300 N.E. Brookwood Parkway
Hillsboro, OR 97124
Phone: (503) 615-9000
FAX: (503) 615-8900

Process Description

TriQuint's TQTRx process is a Gallium Arsenide (GaAs) semiconductor process fabricated at TriQuint's Hillsboro, Oregon facility

The process is an Ion Implanted process combining 0.5 um gate length producing E, D, and D-mode MESFETs ($V_p=100\text{mV}$, -600mV , -2.0V), Schottky diodes, precision NiCr resistors, and MIM capacitors. Includes 2 layers of global, plated Au interconnect, but no Air Bridges.

Product Description

The MESFET power amplifier was designed for 800MHz AMPS and DAMPS applications, using a 4.6V supply voltage. Internal circuitry compensates for temperature and process variations.

Test Plan:

Table 1 lists the qualification plan for TQTRx. This plan is based on the requirements of REL.021

Table 1. Device Qualification Test Plan.

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
MSL	1. Moisture Sensitivity Level Testing		IPC/JESD J-STD-020 Moisture/Reflow Sensitivity Classification of Non-Hermetic Solid State Surface Mount Devices	1 Lot
HTOL	1. Bias Life test	Determine the effect of bias and temp on the device over an extended period of time	JESD22-A108 150°C Junction - 1000 Hours Min	3Lot 77 (1)
Environmental	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	3 Lot 320 (1)
	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	3 Lot 77 (1)
	3. HAST	Determine the effect of temp & humidity on the device under bias.	JESD22-A110 - 96 hr 130°C - 85% RH Non-Condensing	3 Lot 77 (1)
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	3 Lot 77 (1)
Mechanical	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	3 Lot 77 (1)
	2. Physical Dimensions		JESD22-B100-A	3 Lot 15 (0)
	3. Lead Integrity		EIA/JESD22-B105 Cond. A & B (25 leads/Cond)	3 Lot 10
	4. Mark Permanency		EIA/JESD22-B107	3 Lot 25 (1)
	5. Solderability		EIA/JESD22-B102 Cond A	3 Lot 5(0)
ESD	1. ESD Sensitivity	Determine the sensitivity of the device to levels of ESD	HBM per EIA/JESD22-A114	1 Lot 3
	2. ESD Sensitivity		CDM per JESD22-C101	1 Lot 3

Note: HAST, Autoclave, & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

Summary of Results:

Table 2 lists the status and results of the qualification testing for the TQTRx process.

(The present status of the tests is listed in the following section.)

Table 2. Qualification Test Results Summary.

Test Description	Sample Size	Status	Preliminary Lot	Lot #1	Lot #1A	Lot #2	Lot #3
Moisture Sensitivity Level Testing	1 Lot				Passed		
Bias Life test	3Lot 77 (1)			Completed 1,000 hrs. 77/2	Completed 1,000 hrs. 77/0	Completed 1,000 hrs. 77/0	Completed 1,000 hrs. 77/0
PreConditioning	3 Lot 320 (1)		231 / 0	249/3 FA Cracked Die	240/0	240/0	240/0
Autoclave	3 Lot 77 (1)		77 / 0	73/0 1 part lost and 3 part damaged by the handler	77 / 0	77 / 1	77 / 0
HAST	3 Lot 77 (1)		77 / 0	Test Canceled Board Overheated	77/2	77 / 1	77 / 0
Temperature Cycle	3 Lot 77 (1)		77 / 1 (FAR 851)	76/0 1 part lost	77/0	77/0	77/0
Thermal Shock	3 Lot 77 (1)			77/0	77/0	77/0	77/0
Physical Dimensions	3 Lot 15 (0)				Passed	Passed	Passed
Lead Integrity	3 Lot 10				Passed	Passed	Passed
Mark Permanency	3 Lot 25 (1)				Passed	Passed	Passed
Solderability	3 Lot 5(0)				Passed	Passed	Passed
ESD Sensitivity HBM	1 Lot 3		Completed		Passed 300V		
ESD Sensitivity CDM	1 Lot 3		Completed		Passed 600V	Passed 600V	

NOTE: Lot 1A is a replacement lot for #1 which had die cracking

Test Status:

Moisture Sensitivity Level Testing

TQS Test#664

- Procedure: Moisture Sensitivity Level Testing is performed per IPC/JESD J-STD-020.
- Purpose: The purpose of this testing is to identify the classification level of non-hermetic solid state Surface Mount Devices. (Sensitivity of the product / package type to moisture exposure)
- Results: Ten parts from lot 7287 were subjected to level 1 Moisture Sensitivity testing - and all passed electrical test after stress.

HTOL (High Temperature Operating Lifetest)

TQS Test#663, 667, 670, 931

- Procedure: In general, the life test procedure follows MIL-STD-883, Method 1005, Condition B or JESD22-A108.
- Purpose: Life testing is performed for the purpose of demonstrating that device failure rates do not exceed 100 FIT (FIT = Failure unit = failures per billion device hours) for the first 20 years of life at the specified maximum rated operating temperature.
- Results:
- Test 663 has completed 500 hr of HTOL with one failure (FAR 954)
FA determined that the failure was due to EOS.
At 1,007 hrs 1 additional part failed for a random fab defect - Interstage cap short.
 - Test 667 All parts passed after 1,000 hr of HTOL
 - Test 670 All parts passed after 1,000 hr of HTOL
 - Test 931 All parts passed after 1,000 hr of HTOL

◆ Environmental Test Group

Preconditioning

TQS Test#536 & 662, 666, 668, 933

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
- (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
 - (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results:
- Preliminary test 536 (lot 19547) is complete and the 231 parts that were subjected to level 1 preconditioning had no electrical failures.
 - Test 662 (lot 5130) is complete and of 249 parts there were 3 failures. FA indicated that the failures were due to cracked die. This problem has been traced to the assembly facility
 - Test 666 (Lot 6952) is complete an all 240 parts passed electrical test after stress.
 - Test 668 (Lot 7287) is complete an all 240 parts passed electrical test after stress.
 - Test 933 (Lot 7302) is complete an all 240 parts passed electrical test after stress.

Autoclave

TQS Test#536 & 662, 666, 668, 933

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results:
- Preliminary test 536 (lot 19547) is complete and 77 parts were subjected to 96 hr of Autoclave with no electrical failures.
 - Test 662 (lot 5130) 77 parts were subjected to 96 hr of Autoclave with no electrical failures.
One part was lost in the handler and 3 parts were damaged by the handler.
 - Test 666 (Lot 6952) 77 parts were subjected to 96 hr of Autoclave with no electrical failures.

- Test 668 (Lot 7287) 77 parts were subjected to 96 hr of Autoclave with 1 electrical failure.
- Test 933 (Lot 7302) 77 parts were subjected to 96 hr of Autoclave with no electrical failures

HAST (Highly Accelerated Temperature & Humidity Stress Test)

TQS Test#536 & 662, 666, 668, 933

- Procedure: HAST is performed according to JESD22-A110; with the parts biased and an environment of 131°C 85% RH for 96 hrs.
- Purpose: The purpose of the test is to evaluate the reliability of non-hermetic packaged solid state devices in a biased humid environment. This test usually activates the same type of failures as does biased 85/85 but accelerated by temperature, pressure and humidity.
- Results:
- Preliminary test 536 (lot 19547) is complete and 77 parts were subjected to 96 hr of HAST with no electrical failures.
 - Test 662 (Lot 5130) is complete - The board and the parts overheated and were damaged.
 - Test 666 (Lot 6952) 75 of 77 parts passed electrical test.
Two (2) parts failed for random fab defects that caused capacitor shorts.
 - Test 668 (Lot 7287) 77 parts were subjected to 96 hr of HAST with 1 electrical failure.
 - Test 933 (Lot 7302) 77 parts were subjected to 96 hr of HAST with no electrical failures

Temperature Cycle

TQS Test#536 & 662, 666, 668, 933

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results:
- Test 536 (lot 19547) is complete 77 parts were subjected to 1,000 temperature cycles from -40°C to +125°C - One electrical failure was detected after 1,000 cycles. Failure analysis (FAR 851) indicated that the failure was related to degradation of a FET..
 - Test 662 (Lot 5130) complete 1,000 cycles - One (1) part was lost in the handler - the remaining 76 parts all passed.
 - Test - 666 (Lot 6952) completed 1,000 cycles with no failures.
 - Test - 668 (Lot 7287) completed 1,000 cycles with no failures.
 - Test - 933 (Lot 7302) completed 1,000 cycles with no failures.

◆ Mechanical Test Group

Thermal Shock (Liquid to Liquid)

TQS Test# 665, 669, 671, 932

- Procedure: The test shall be performed according to JESD22-A106 Condition C except -40°C to +125°C
- Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.
- Results:
- Test 663 (Lot 5130) was subjected to 100 cycles between -40°C to +125°C with no electrical failures.
 - Test 665 (Lot 5130) was subjected to 100 cycles between -40°C to +125°C All 77 Passed
 - Test 669 (Lot 6952) was subjected to 100 cycles between -40°C to +125°C All 77 Passed
 - Test 671 (Lot 7287) was subjected to 100 cycles between -40°C to +125°C All 77 Passed.
 - Test 932 (Lot 7302) was subjected to 100 cycles between -40°C to +125°C All 77 Passed.

Physical Dimensions

TQS Test# 669, 671, 932

- Procedure: The test shall be performed according to JESD22-B100.
- Purpose: The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable documents.
- Results:
- Test 669 (Lot 6952) - Passed
 - Test 671 (Lot 7287) - Passed
 - Test 932 (Lot 7302) - Passed

Lead Integrity

TQS Test# 669, 671, 932

- Procedure: The test shall be performed according to JESD22-B105 Cond. A & B.
- Purpose: The purpose of the test is to determine the integrity of the lead/package interface and the lead itself where the lead(s) are bent due to faulty board assembly followed by rework of the parts for re-assembly
- Results: - Test 669 (Lot 6952) - Passed
- Test 671 (Lot 7287) - Passed
- Test 932 (Lot 7302) - Passed

Marking Permanency

TQS Test# 669, 671, 932

- Procedure: The test shall be performed according to JESD22-B107.
- Purpose: The purpose of the test is to verify that the markings on the device will not become illegible when subjected to solvents of cleaning solutions commonly used during the removal of solder flux residue from the board assembly process
- Results: - Test 669 (Lot 6952) - Passed
- Test 671 (Lot 7287) - Passed
- Test 932 (Lot 7302) - Passed

Solderability

TQS Test# 669, 671,932

- Procedure: The test shall be performed according to JESD22-B102.
- Purpose: The purpose of this test is to provide a means of determining the solderability of devices package terminations that are intended to be joined to another surface using solder for the attachment.
- Results: - Test 669 (Lot 6952) - Passed
- Test 671 (Lot 7287) - Passed
- Test 932 (Lot 7302) - Passed

◆ ESD Test Group

ESD Testing (HBM)

TQS Test#703,

- Procedure: This testing will be performed per EIA/JESD22-A114
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic HBM discharge.
- Results: ESD testing on Lot# 1 completed. Pin4 (Gnd) to Pin11 (RFoutD) Failed at +400V
Pin2 (VregA) to Pin1 (Vds1A) Failed at +500V
Pin2 (VregA) to Pin8 (Vds1D) Failed at +500V
Pin7 (VregD) to Pin11 (RFoutD) Failed at +500V
All remaining pin combinations exceeded 500V

ESD Testing (CDM)

TQS Test# 934, 935

- Procedure: This testing will be performed per EIA/JESD22-C101
- Purpose: The purpose of this testing is to classify the device according to its susceptibility to damage or degradation by exposure to a defined electrostatic CDM discharge.
- Results: Parts from lot 7287 were subjected to CDM ESD and all passed at 600V.
Parts from lot 7302 were subjected to CDM ESD and all passed at 600V.

□ **Conclusion**

The TQTRx process has successfully completed all reliability testing per the requirements specified in REL.021 and is now considered to be qualified.