Sigma Metallization System Qualification Report

Abstract

This report summarizes the reliability testing that has been completed to qualify the Sigma metallization system for use in TriQuint wafer fabrication - a down converter product was used as the qualification vehicle.

The Down Converter used as the test vehicle was fabricated on TriQuint's 1.0µm E/D MESFET GaAs and is packaged in a QSOP-16 package. Assembly and encapsulation of the test samples were accomplished at supplier U. Tests, test sample size and failure criteria were defined from TriQuint’s Specification REL.021 (Policy and Procedure for Reliability Qualifications of ICs). Most tests outlined in this procedure follow the JEDEC Standard Number 26-A or MIL-STD-883 when applicable.

NOTE: This test also qualified the QSOP-16 package from Assembly Vendor U and the QED2 process

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Process Description

TriQuint's QED2 process is a Gallium Arsenide (GaAs) semiconductor process fabricated at TriQuint's Hillsboro, Oregon facility. The process is an Ion Implanted process combining 1.0 and 0.5 µm MESFETs, Schottky diodes, precision NiCr resistors, MIM capacitors and airbridge inductors. The process includes 2 layers of global plated Au interconnect.

Product Description

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Down Converter

The downconverter used as a test vehicle is a 3 volt receiver RFIC designed specifically for TDMA IS-136 applications. The product contains a down converter and LNA circuits for the 800 MHZ cellular band. The mixer uses a high-side LO frequency with the IF covering a range of 85-120 MHZ.

Sigma Metallization System Qualification

Reliability Test Report 11/15/99

Test Plan:

The down converter was assembled in a QSOP-16 package by supplier U. Conductive epoxy is used as the die attach and 1.0 mil gold bond wires are used to bond the circuit to the package leadframe. The wafers used to produce this produce were processed using the Sigma Field Metallization system

Table 1. Process Qualification Test Plan.

Item #	Test Name	Purpose	Specification - Method or Conditions	Sample Size
1	IR Reflow Simulation	Determine the effect of repeated IR Reflow temperatures stress on the device	J-STD-020 235°C +5/-0 Peak Temperature 12 IR Reflow simulations	2 Lots 200/1
2	Tempermal Shock (Liquid to Liquid)	Determine the effect of temp on Material Thermal Mismatch	JEDEC A106, Condition D -65°C to +150°C 100 Cycles	2 Lots 200/1
3	Temperature Cycle (Air to Air)	Determine the effect of temp on Material Thermal Mismatch	-40°C to +125°C, for 1,000 Cycles JEDEC STD 22, Method A104, Condition G	2 Lots 77/1
4	AutoClave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	2 Lots 77/1
5	HAST	Determine the effect of temp & humidity on the device under bias	JEDEC A110, Condition C 130oC, 85% RH for 33.5 PSIA 96 Hours VDD biased at 5.0V	2 Lots 77/1
6	HTOL Life test	Determine the effect of bias and temp on the device over an extended period of time	VDD biased at 2.8 V 1,000 hrs Ambient Temperature, 125°C	2 Lots 77/1

Note: HAST, Autoclave, & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

Test Status:

Preconditioning

Procedure: Devices belonging to the HAST, Autoclave and Temperature Cycle groups were preconditioned to level 1 requirements prior to beginning their respective stresses. They first received a stabilization bake for 24 hours @ 125°C, followed by an unbiased temperature and humidity soak at 85°C/85% humidity for 168 hours and, finally by 3 cycles of IR reflow. This preconditioning was performed according to JEDEC Methods A101 & A113.

Purpose: The purposes of preconditioning are:

(1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
(2) to determine if the solder reflow will have any long-term effect on reliability.

Thermal Shock (Liquid to Liquid)

TQS Test# 474 & 476

Lot# 2816 & 2817 - Two Hundred (200) parts from each lot were placed in Liquid to Liquid Thermal Shock - JEDEC A106 Condition D (-65°C to +150 °C for 100 cycles).
Testing was performed after 100 cycles - All Parts Passed Electrical Test

Temperature Cycle (Air to Air)

TQS Test# 481 & 482

Lot# 2816 - Seventy seven (77) parts were placed in Air to Air Thermal cycle JEDEC STD 22, Method A104 ,Condition G (-40°C to +125 °C).
Testing was performed after 500 & 1,000 cycles
- One (1) part failed after 500 cycles due to a VIA failure (FAR 688)
- One (1) part failed after 1,000 cycles due to ESD (FAR 704)

Lot# 2817 - Seventy seven (77) parts were placed in Air to Air Thermal cycle JEDEC STD 22, Method A104 ,Condition G (-40°C to +125 °C).
Testing was performed after 500 & 1,000 cycles
- One (1) part failed after 1,000 cycles due to a VIA failure (FAR 705)

Autoclave

TQS Test# 481 & 482

Lot# 2816 & 2817 - Seventy seven (77) parts from each lot were placed in 121°C, 100% RH, 15 PSIA autoclave for 96 hrs. JEDEC A102, Condition C unbiased, for 96 Hours -
All Parts Passed Electrical Test

HAST

TQS Test# 481 & 482

Lot# 2816 & 2817 – Seventy seven (77) parts from each lot were placed in HAST JEDEC A110, Condition C - 130°C, 85% RH for 33.5 PSIA VDD biased at 2.8V for 96 hrs.
All Parts Passed Electrical Test

HTOL (Life Test @ 125°C) TQS Test# 484 & 485

Seventy seven (77) parts from each lot were placed in 125°C ambient under bias of 2.8 volts. Parts were tested after 250, 500 and 1,000 hrs.

Lot# 2816 - One (1) part was lost in the handler after 250 hrs of HTOL. The remaining 76 parts passed all electrical tests after 250, 500 & 1,000 hrs of HTOL.

Lot# 2817 One (1) part failed for a shorted capacitor after 250 hrs of HTOL. (FAR 699) The remaining 76 parts passed all electrical tests after 250, 500 & 1,000 hrs of HTOL.

Summary:

There were no reported failures during the following tests:

- **Preconditioning**
- **Thermal Shock**
- **Autoclave**
- **Hast**

There were reported failures during the following tests:

- **Temperature Cycle:**
  - There was one (1) failure reported after 1,000 cycles on Lot# 2817
    - It was determined to be a open VIA. (FAR 705)
  - There were two (2) failure reported on Lot# 2816
    - There was one (1) failures after 500 cycles that was determined to be an open VIA. (FAR 688)
    - There was one (1) failures after 1,000 cycles that was determined to be due to ESD (FAR 704) - therefore was not counted as a stress failure.
- **HTOL Testing:**
  - There were one (1) failure reported after 250 hrs of HTOL on Lot# 2817
    - It was determined to be a shorted capacitor (FAR 669).

All of the tests specified in the test plan were successfully completed