

# TQ-9222

## Reliability Monitor Testing

### Abstract

This report summarizes the reliability testing that has been completed to monitor the reliability of the TQ-9222 product.

The TQ-9222 is fabricated on TriQuint's 0.6 $\mu$ m E/D MESFET GaAs and is packaged in a QSOP-24 package. Assembly and encapsulation of the test samples were accomplished at supplier U. Tests, test sample size and failure criteria were defined from TriQuint's Specification REL.021 (Policy and Procedure for Reliability Qualifications of ICs). Most tests outlined in this procedure follow the JEDEC Standard Number 26-A or MIL-STD-883 when applicable.

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## Process Description

TriQuint's TQTRx process is a Gallium Arsenide (GaAs) semiconductor process fabricated at TriQuint's Hillsboro, Oregon facility

## Product Description

TQ9222 is a 3-V, RF receiver IC designed specifically for dual-band TDMA applications. Its RF performance meets the requirements of products designed to the IS-136 and GSM standards.

The TQ9222 contains two separate LNA+Mixer circuits to handle both the 800 MHz cellular band and the 1900 MHz PCS band. The mixers use a high-side LO frequency, with the IF covering a range of 70-140 MHz. The IF frequencies below 120 MHz are possible due to the 1/2 -IF spurious signal rejection in the 1900 MHz LNA+Mixer. The IF outputs are designed for use of a common IF frequency. Most RF ports are internally matched to 50 Ohms, greatly simplifying the design and keeping the number of external components to a minimum. Separate supply voltage connections provide the required flexibility for dual-band operation. The TQ9222 achieves good RF performance with low current consumption, supporting long standby times in portable applications. Coupled with the very small QSOP24 package, the part is ideally suited for dual-band mobile phones.

**Test Plan:**

The TQ-9222 is a standard product that is manufactured on the TQTRx process from the Hillsboro, Oregon facility and is packaged in a QSOP-24 Plastic Package.

**Test Plan:**

Table 1 lists the monitor plan for TQ9222. This plan is based on the requirements of REL.021

**Table 1. Device Qualification Test Plan.**

	Test Description	Purpose	Specification - Method or Conditions	Sample Size
<b>HTOL</b>	1. Bias Life test	Determine the effect of bias and temp on the device over an extended period of time	JESD22-A108 150°C Junction - 1000 Hours Min	1 Lot 77 (1)
	1. PreConditioning		JESD22-A113 IR/Convection Reflow @ 235°C	240 (1)
<b>Environmental</b>	2. Autoclave	Determine the effect of temp, humidity & pressure on the device over time, unbiased.	JEDEC A102, Condition C 121°C, 100% RH, 15 PSIA unbiased, for 96 Hours	1 Lot 77 (1)
	3. HAST	Determine the effect of temp & humidity on the device under bias.	JESD22-A110 - 96 hr 130°C - 85% RH Non-Condensing	1 Lot 77 (1)
	4. Temperature Cycle	Determine the effect of temp on Material Thermal Mismatch.	JESD22-A104 Cond G -40°C to +125°C 1000 Cycles	1 Lot 77 (1)
<b>Mechanical</b>	1. Thermal Shock	Determine the effect of temp on Material Thermal Mismatch.	Similar to JESD22-A106 Cond. C <i>except</i> -40°C to +125°C - 100 Cycles	1 Lot 77 (1)
	2. Physical Dimensions		JESD22-B100-A	1 Lot 15 (0)
	3. Lead Integrity		EIA/JESD22-B105 Cond. A & B (25 leads/Cond)	1 Lot 1
	4. Mark Permanency		EIA/JESD22-B107	1 Lot 25 (1)
	5. Solderability		EIA/JESD22-B102 Cond A	1 Lot 5(0)

Note: HAST, Autoclave, & Temperature Cycle groups received preconditioning. Please see description of preconditioning stresses.

## Summary of Results:

Table 2 lists the status and results of the qualification testing for TQ-9222.

*(The present status of the tests is listed in the following section.)*

**Table 2. Qualification Test Results Summary.**

Test Description	Sample Size	Status	
Bias Life test	1 Lot 77 (1)	77 parts were subjected to 1,000 hr of HTOL testing. All 77 parts passed electrical testing at 500 hr and 1,000 hr.	77(0)
PreConditioning	1 Lot 249 (1)	249 parts were subjected to level 1 Preconditioning and all passed electrically after the stress test.	240(0)
Autoclave	1 Lot 77 (1)	All 77 parts passed	77(0)
HAST	1 Lot 77 (1)	All 77 parts passed	77(0)
Temperature Cycle	1 Lot 77 (1)	74 parts passed electrical test after stress - 3 parts were damaged by ESD.	74(0)
Thermal Shock	1 Lot 77 (1)	All parts passed	77(0)
Physical Dimensions	1 Lot 15 (0)	All parts passed	15/(0)
Lead Integrity	2 Lot 10	All parts passed	10/(0)
Mark Permanency	2 Lot 25 (1)	All parts passed	25/(0)
Solderability	2 Lot 5(0)	All parts passed	5/(0)

**HTOL (High Temperature Operating Lifetest)**

TQS Test# 1019

- Procedure: In general, the life test procedure follows MIL-STD-883, Method 1005, Condition B or JESD22-A108.
- Purpose: Life testing is performed for the purpose of demonstrating that device failure rates do not exceed 100 FIT (FIT = Failure unit = failures per billion device hours) for the first 20 years of life at the specified maximum rated operating temperature.
- Results: 77 parts from lot 7604 were subjected to 1,000 hr of HTOL stress. All parts pass electrical test after 500 and 1,000 hr.

**◆ Environmental Test Group****Preconditioning**

TQS Test# 1020

- Procedure: Preconditioning is performed according to JEDEC Methods A101 & A113.
- Purpose: The purposes of preconditioning are:
- (1) to determine if any trapped moisture around the device leads will explode the plastic around the leads (popcorning) or cause delamination of the plastic from the chip during the soldering process.
  - (2) to determine if the solder reflow will have any long-term effect on reliability.
- Results: 240 parts from lot 7604 were subjected to level 1 preconditioning with no electrical failures.

**Autoclave**

TQS Test# 1020

- Procedure: Un-Biased Autoclave is performed per JESD22-A102
- Purpose: The purpose of unbiased autoclave (Accelerated Moisture Resistance Test) is to evaluate the moisture resistance of non-hermetic packaged solid state devices.
- Results: 77 parts from lot 7604 were subjected to 96 hr of Autoclave - All passed electrical test.

**HAST (Highly Accelerated Temperature & Humidity Stress Test)**

TQS Test# 1020

- Procedure: HAST is performed according to JESD22-A110; with the parts biased and an environment of 131°C 85% RH for 96 hrs.
- Purpose: The purpose of the test is to evaluate the reliability of non-hermetic packaged solid state devices in a biased humid environment. This test usually activates the same type of failures as does biased 85/85 but accelerated by temperature, pressure and humidity.
- Results: 77 parts from lot 7604 were subjected to 96 hr of HAST - All passed electrical test.

**Temperature Cycle**

TQS Test# 1020

- Procedure: Temperature cycle is performed according to JESD22-A104 Condition G, -40°C to +125°C, for 1000 cycles.
- Purpose: The purpose of the test is to determine the resistance of the part to extremes of high and low temperature and the effect of alternate exposures to these extremes.
- Results: 77 parts from lot 7604 were subjected to 1,000 temperature cycles from -40°C to +125°C. Three (3) parts failed due to ESD - the remaining 74 parts passed all electrical tests.

**◆ Mechanical Test Group****Thermal Shock (Liquid to Liquid)**

TQS Test# 1021

- Procedure: The test shall be performed according to JESD22-A106 Condition C except -40°C to +125°C.
- Purpose: The purpose of the test is to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the affect of alternate exposures to these extremes.
- Results: 77 parts from lot 7604 were subjected to 100 thermal shock cycles between -40°C to +125°C. All parts passed electrical test.

**Physical Dimentions**

TQS Test# 1021

- Procedure: The test shall be performed according to JESD22-B100.
- Purpose: The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable documents.
- Results: 15 parts from lot 7604 were subjected to Physical Dimension verification with no failures.

**Lead Integrity**

TQS Test# 1021

- Procedure: The test shall be performed according to JESD22-B105 Cond. A & B.
- Purpose: The purpose of the test is to determine the integrity of the lead/package interface and the lead itself where the lead(s) are bent due to faulty board assembly followed by rework of the parts for re-assembly.
- Results: Two groups of 25 leads (5 parts) from lot 7604 were subjected to lead integrity testing (Condition A and B) with no failures.

**Marking Permanency**

TQS Test# 1021

- Procedure: The test shall be performed according to JESD22-B107.
- Purpose: The purpose of the test is to verify that the markings on the device will not become illegible when subjected to solvents of cleaning solutions commonly used during the removal of solder flux residue from the board assembly process.
- Results: 25 parts from lot 7604 were subjected to marking permanency testing with no failures.



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**Solderability**

TQS Test# 1021

Procedure: The test shall be performed according to JESD22-B102.

Purpose: The purpose of this test is to provide a means of determining the solderability of devices package termination's that are intended to be joined to another surface using solder for the attachment.

Results: 25 leads (5 parts) from lot 7604 were subjected to solderability testing with no failures.

**□ Conclusion**

The TQ9222 produced on the TriQuint 0.6 $\mu$ m E/D MESFET process and assembled in a QSOP-24 package built by subcontractor U has successfully passed the reliability monitor during the Third Qtr of 2000.