Probe Based Simulation Technique for Modeling Saturated Power Amplifiers

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Abstract—**This paper describes a probe based analysis technique for the simulation of saturated power amplifiers. The method is in-situ, compatible with linear & nonlinear simulation and accounts for the impact of network symmetry on the performance of the circuit. The load impedance is determined for every transistor cell in the circuit enabling the calculation of output power, network loss and drive margin for the entire amplifier. The technique is applied to a binary manifold typical of high frequency amplifiers, as well as a single stage GaN x-band high power amplifier design. Measured results for the GaN power amplifier at 9.4GHz under continuous wave conditions demonstrate 41.6W output power with associated gain and power added efficiency of 9.5dB and 44% respectively.**

Keywords-saturated power amplifiers, Gallium Nitride, load pull, Cripps's method

I. INTRODUCTION

In contrast to linear components intended for communication systems, many applications require that the power amplifier (PA) operate under saturated conditions. Available nonlinear transistor models often prove to be difficult to use for saturated power amplifier design and optimization. Reasons include but are not limited to model inaccuracy, unknown harmonic terminations at high frequency and convergence issues for multiple cell designs under large signal conditions. On the other hand, measured load pull data partnered with judicious use of small signal linear models has been demonstrated to produce accurate results and for many is the preferred approach to saturated power amplifier design. Load pull based approaches to power amplifier design are often referred to as Cripps's methods based on the analysis first described in reference [1].

Standard implementations of the Cripps's method require that each stage of the circuit be separated from one another. This is not only cumbersome and prone to error, but it breaks potential feedback loops that may influence the impedances present in the actual circuit. Stages that use multiple transistor cells are analyzed by connecting the matching network manifold ports together in parallel. Doing this inherently assumes that the output manifold is symmetric and that all of the transistors are equally driven by the input matching network in a purely even mode of operation. Most real manifolds however are not perfectly symmetric and analyzing the structure with all of the ports connected together will yield the average load impedance presented to the transistors. Optimizing this impedance to conjugate match the measured load pull data will not guarantee that the individual transistor cells are optimally loaded. Furthermore, any asymmetry in the input matching network will result in the transistors not being evenly driven, exciting an odd-mode component and current imbalance between the cells. This imbalance will manifest itself in nonuniform loading of the transistor cells.

This paper describes a probe based analysis technique that is compatible with the Cripps's methodology, however allows for the determination of individual transistor cell load impedances under the correct mode of operation without separating the circuit. The overall impact of network asymmetry on transistor output power and network loss is properly accounted for and thus may be minimized as part of the design process.

II. DESCRIPTION

The method described in the remainder of this paper is straightforward to implement within standard microwave simulation tools, however it is required that load pull data be available for the transistor cells under consideration. Specifically, the optimum load Z_{LP} , and the corresponding output power, P_{LP}. The device output is modeled as a parallel RC equivalent circuit with the following element values.

$$R_p = 1/\mathrm{Re}\{1/Z_{LP}^*\} \quad (1)$$

$$C_p = \mathrm{Im}\{1/Z_{LP}^*\}/\omega \quad (2)$$

Next, place current and voltage probes at the input and output each transistor model in the circuit as shown in Figure 1.

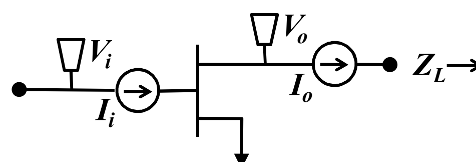

Figure 1. Current and voltage probe placement.

The device model can be linear or nonlinear, however, it will be assumed to be a linear model for the balance of this paper.

In order to measure the complex fundamental frequency current and voltage, a test signal must be applied at the input port of the circuit. It is convenient to use a harmonic balance source set to 0dBm as the test signal. Since the entire circuit is linear, the harmonic number can be set to unity minimizing the impact on simulation time. For every transistor in the circuit complex current and voltage signals are determined and the following parameters calculated within the output equation block of the simulation tool.

$$Y_L = I_o / V_o + j\omega C_p \tag{3}$$

$$P_i = \mathrm{Re}\{V_i I_i^*\}/2 \tag{4}$$

$$P_o = \mathrm{Re}\{V_o I_o^*\}/2 \tag{5}$$

Note that for (3) the capacitance of the transistor output equivalent circuit has been absorbed into the load admittance. Bear in mind that (4) and (5) represent test signal power, not the actual RF power for the amplifier. The actual transistor RF output power is estimated with the Cripps's method using load pull data for the transistor cell [1].

$$P_{out} = \min\left\{ \mathrm{Re}\left(P_{LP} R_P Y_L^*\right), \mathrm{Re}\left(\frac{P_{LP}}{Y_L R_P}\right) \right\} \tag{6}$$

To illustrate how one uses this data consider the multistage, multicell power amplifier example shown in Figure 2.

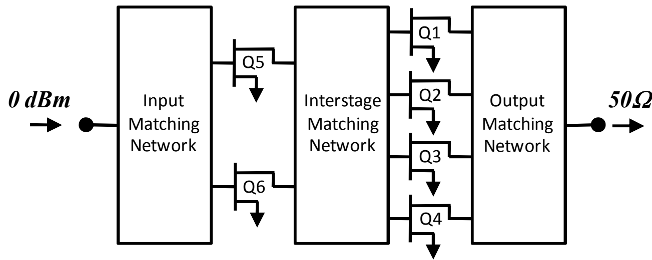

Figure 2. 2-Stage power amplifier example.

The test signals can be used to calculate network losses and output stage gain. Since test signal applied to the input is 0dBm, the test signal power at the output will be equal to the simulated gain of the circuit, S_{21}. It is simply a matter of summing the test signal powers at the appropriate locations in the circuit to compute the following.

$$L_{OMN}(dB) = S_{21}(dB) - 10\log\left(\sum_{n=1}^{4} P_{o,n}\right) \tag{7}$$

$$L_{ISMN}(dB) = 10\log\left(\sum_{n=1}^{4} P_{i,n}\right) - 10\log\left(\sum_{n=5}^{6} P_{o,n}\right) \tag{8}$$

$$G_{Stg2}(dB) = S_{21}(dB) - 10\log\left(\sum_{n=5}^{6} P_{o,n}\right) - G_c(dB) \tag{9}$$

The gain compression level for the output stage, $G_c(dB)$ is estimated as the compression level observed for the load pull data. The RF output power for the circuit will be the sum of the stage-2 transistor output power as computed with (6) less the output matching network loss (7).

$$P_{RF}(dBm) = 10\log\left(\sum_{n=1}^{4} P_{out,n}\right) + L_{OMN}(dB) \tag{10}$$

The ability for stage-1 to drive the output stage, otherwise known as the drive margin is calculated as follows.

$$dM(dB) = 10\log\left(\sum_{n=5}^{6} P_{out,n}\right) + G_{Stg2}(dB) - P_{RF}(dBm) \tag{11}$$

III. Circuit Simulation Examples

The first example concerns the analysis of network symmetry. The structure shown in Figure 3 is common in millimeter-wave power amplifier MMICs. Two HV15 PHEMT cells are connected with a binary combining structure and an odd mode suppression resistor between the drain feeds. Measured load pull data under efficiency tuned conditions for this process demonstrates 1100mW/mm output power at 35GHz for an 8V drain bias [2]. Input and output feed structures are EM simulated and the output termination was optimized for maximum output power at 35GHz. This network is clearly symmetric and both FETs are predicted to have identical output power achieving 1100mW/mm at 35GHz.

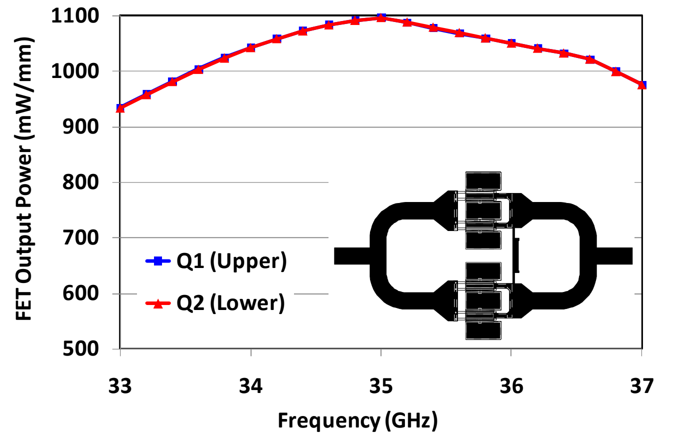

Figure 3. HV15 FETs with symmetric input and output feeds.

If the FET pair is to be connected to an adjacent pair, a 90º bend might be added to the output network as shown in Figure 4. The output termination was re-optimized for maximum power at 35GHz. Due to current crowding, mode formation, etc., the addition of the bend has induced asymmetry in the output network reducing the FET cell output power by 0.34dB. Things are actually worse, now there is power dissipation in the odd mode suppression resistor and an additional 0.38dB of effective loss for the output network. To minimize parasitic

effects odd mode suppression resistors are commonly made to be physically small. It is quite possible that enough imbalance could damage these resistors.

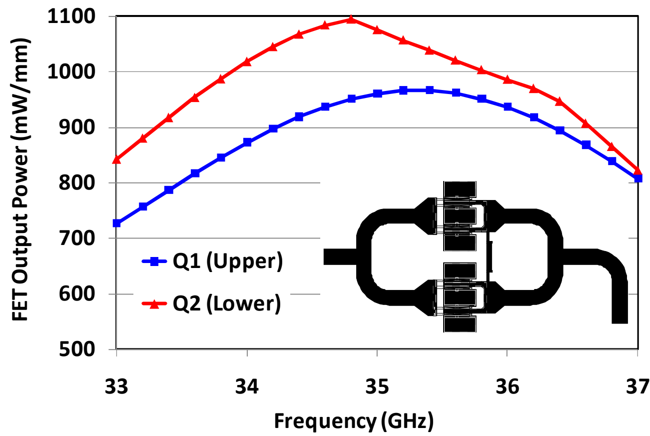

Figure 4. Symmetric input feed and bend at output feed.

Asymmetry in the input network can imbalance the FET input drive levels which will in turn cause imbalanced signals at the FET outputs. The situation depicted in Figure 5 has a symmetric output network with a 90º bend placed at the input. Again optimizing the load for maximum power a higher degree of imbalance is predicted for the asymmetric input than what was projected for an asymmetric output. The FET output power is reduced by -0.46dB. In other words, input network asymmetry can alter the output load presented to the transistors. One also must take care when parsing a large network into smaller EM simulation blocks. If the bend and tee are not EM simulated together, the impact of the bend on circuit imbalance will be lost.

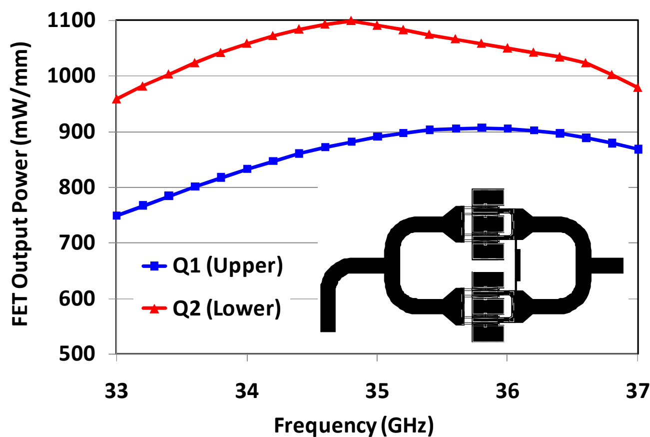

Figure 5. Curve at input feed and symmetric output feed.

As a second example the proposed method is used to design a single stage x-band power amplifier circuit utilizing TriQuint Semiconductor TGF2023-10 discrete GaN FETs [3]. This 10mm total periphery device is constructed of 8 x 1.25mm unit FET cells. A 16 port s-parameter file for TGF2023-10 transistor under small signal conditions is available on-line. The layout and s-parameter file configuration for the TGF2023-10 is shown in Figure 6. Current and voltage probes are attached to each gate/drain port pair to simulate the loading of the unit FET cells.

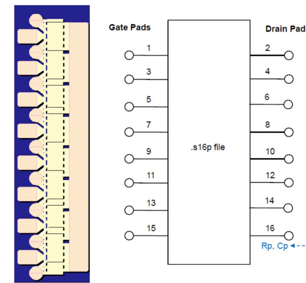

Figure 6. TGF2023-10 GaN FET and on-line s-parameter model.

A photograph of the constructed amplifier is shown in Figure 7. The input and output matching network material is 5mil thick polished alumina with 8µm thick gold metallization. The various components are soldered to a 40mil thick CuMo carrier plate. The assembled carrier plate is mounted to an aluminum test fixture and the RF ports contacted with connectorized launchers. The matching networks were EM simulated with Sonnet^{TM} featuring individual ports for each bondwire connection. The entire amplifier circuit was analyzed with AWR Microwave Offce^{TM} utilizing the quasi-EM based multiple bondwire model (BWIRES2) resident in the simulation tool [4].

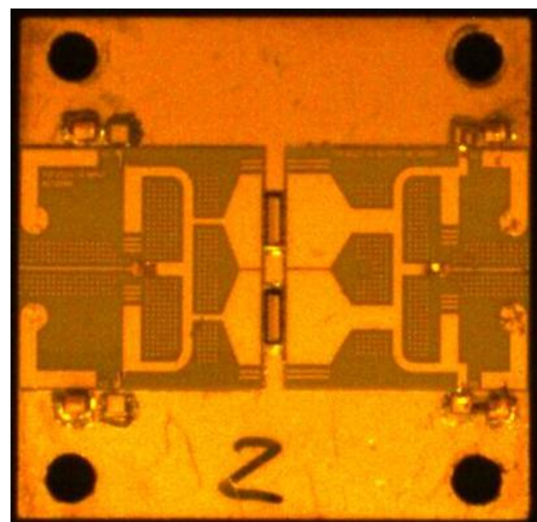

Figure 7. TGF2023-10 x-band power amplifier.

The initial simulations for the transistor connected with minimum length bondwires predicted that the transistor output connections would be not be uniformly loaded. The distribution of output impedances for the eight connection

points is shown in Figure 8. Note that C_p has been absorbed in the output network. The output ports experience uniform loading with respect to the die symmetry line (squares and X of the same color), however the pairs vary significantly from one another and are not centered on the real axis. The output bondwire configuration can be altered to compensate for this effect. Placing the bondwires at increasing angles as shown in Figure 9 significantly improves the load imbalance. The simulated loading for the angled bondwire configuration is plotted in Figure 10. The load impedances are much more uniform and are centered on the real axis.

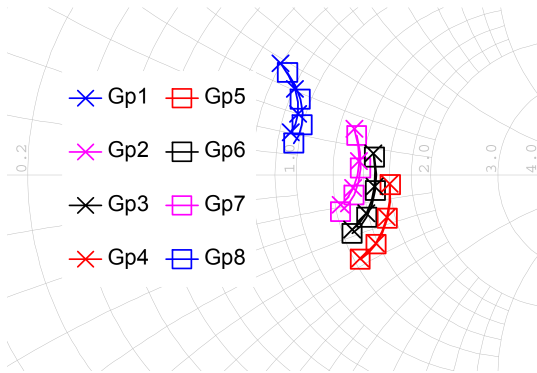

Figure 8. Output loading for minimum length bondwires.

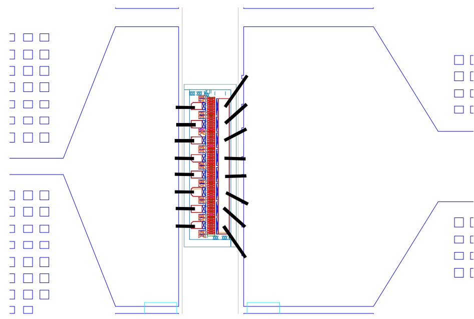

Figure 9. Compensation with flared bondwires.

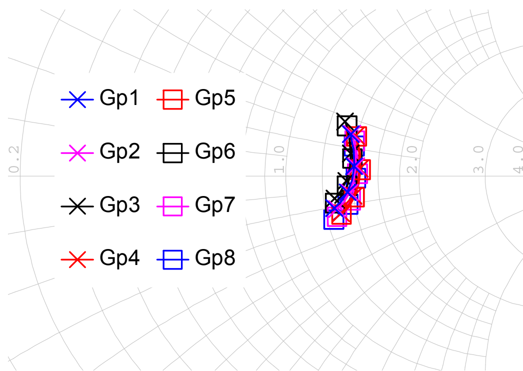

Figure 10. Output loading with bondwire compensation.

Measured in-fixture results at for the dual TGF2023-10 power amplifier at 9.4GHz are shown in Figure 11. The data was collected under CW conditions at room temperature for a 30V drain bias. The peak power added efficiency was observed to be 44% with associated output power and gain of 46.2dBm and 9.5dB respectively.

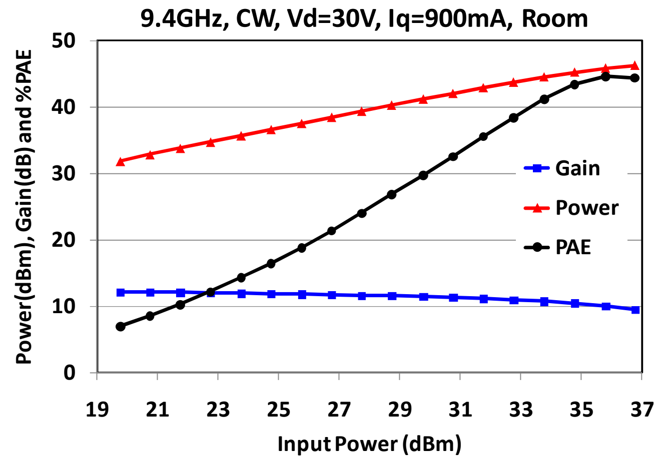

Figure 11. Measured CW results for the TGF2023-10 amplifier.

Conclusion

A probe based analysis technique for the simulation of saturated power amplifiers has been presented. The method is in-situ and allows one to properly estimate and impact network symmetry on the output power of the circuit. The technique was first applied to a binary manifold, demonstrating the impact of asymmetry for both the input and output matching networks. A second example described the design of a single stage x-band high power amplifier using TriQuint Semiconductor TGF2023-10 discrete FETs. Measured CW results for the power amplifier at 9.4GHz demonstrate 41.6W of output power with associated power gain and power added efficiency of 9.5dB and 44% respectively.

References

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