

# High Efficiency, Wide Band 50 Watt, 28V InGaP/GaAs HBT MMIC

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**Abstract**— This paper reports on a 50W high efficiency wide band InGaP/GaAs high voltage HBT (HVHBT) two stage MMIC operating at 750MHz to 960MHz. It uses a high breakdown voltage, high ruggedness HBT process developed by TriQuint Semiconductor. The device employs a temperature compensation bias circuit to stabilize bias current change over temperature. The P-1dB of the device reaches 47dBm (50W), with a gain of around 31dB, collect efficiency of 65% . Test with a DPD (digital pre-distortion) system, this MMIC can reach ACLR of -57dBc at Pout=41dBm with collect efficiency of 36% for WCDMA two carriers modulation signal (PAR=6.5dBc, 2c0110 signal configuration).

## I. INTRODUCTION

The application of InGaP/GaAs HVHBTs for base station infrastructure applications operating at 28V obtained more attention recently[1]-[3] because of its inherent superiority in linearity and efficiency [4]-[6].

In the past, MMIC drivers were designed to optimize both linearity and efficiency. With digital pre-distortion (DPD) circuits being widely used for the linearity improvement of power amplifiers, linearity is no more a key factor to limit power amplifier to be used in infrastructure applications. Instead, high efficiency power amplifiers become more important in “green base-station” applications.

In this paper we report for the first time a single chip 50W 2-stage HVHBT MMIC operating at 28V with an excellent linearity and efficiency.

## II. HVHBT FABRICATION

For 28V operation, InGaP/GaAs HBTs use thick collectors for high breakdown voltages. Typical BVcbo’s are more than 70V, and BVceo’s are higher than 40V. Although thick collectors present process challenges, the devices are extremely reliable and rugged. Over 3000 hours of lifetime at an accelerated stress test at 315oC junction temperature was achieved. [5], [7], [8]. MMIC for HVHBT was achieved with 2 interconnection metal layers, MIM capacitors, thin film resistors, spiral inductors, and through substrate via holes. The substrate was thinned to 4 mils before packaging. Because of the large chip size and the existence of via holes, special cares were taken during packaging to ensure good electrical and thermal contact

## III. TWO STAGES HIGH POWER HBT MMIC DESIGN

High power HBT, like any other semiconductor technology, is made of multiple small devices strung together in parallel. Certain numbers of fingers make up a basic building block, and high power MMICs are composed of many building blocks parallels together.

In this work, we design a two stages 50W MMIC. The first stage has two basic building blocks, the second stage 50W device was built by paralleling sixteen identical building blocks, with each delivering 3.5W and consisting of 16 transistor fingers. Each building block is accompanied by an on-chip MMIC pre-matching circuit. Fig. 1 shows the photograph of a completed chip, which measures 3.7mm by 5.56mm.

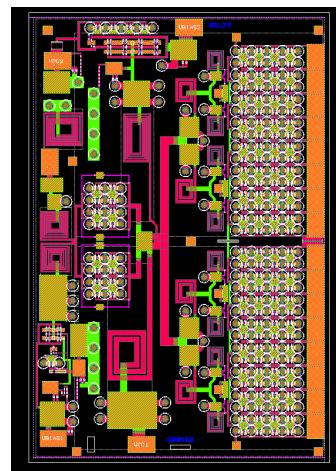


Fig. 1 50W Two Stages TriPower MMIC Die layout

For a high power MMIC design, one of the most important considerations is the thermal management. From a given specification of the highest junction temperature in real application, we need to select the finger size, finger to finger and row to row space with right numbers by using thermal simulation and measurement [9]. To improve device stability and the safe operating area (SOA), we have chosen a proper ballast resistor for each finger [10]. However, detailed simulation has to be performed to trade off the device stability

and the degradation in device performance due to the use of high ballast resistors

For large size transistors, the signal uniformity along each row and between different building blocks is extremely important. EM simulation was performed to determine the differences in the signal's phase and magnitude between different fingers, rows and building blocks. The feeds of the signal lines were then carefully designed to ensure the balance in signal distribution. There is also a tradeoff between the chip's vertical and the horizontal dimensions for signal uniformity.

The bias circuit for the 28V power HVHBT is implemented on the same chip using a current mirror circuit. An excellent thermal stability is achieved with less than 5% change in the quiescent current over the temperature range from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . A power down feature is available through a pin providing the reference current into the bias circuitry. Fig. 2 shows the schematic of this 50W two stage MMIC.

For base station applications, linearity is one of the most important factors determining the usefulness of a power amplifier. For HBTs, there are many factors that can affect the overall device linearity [11]-[13]. From the application point of view, the bias condition and the source and the load impedances of a device all can have a large impact on its ACPR. The influence of the load impedance is especially strong for class AB applications. The load pull results show, the optimized  $Z_{load}$ 's of best ACPR, best gain and best efficiency are not the same, but form a triangle in the Smith chart [4]. For real applications, one has to evaluate the tradeoffs among the various performance requirements to choose the proper impedance

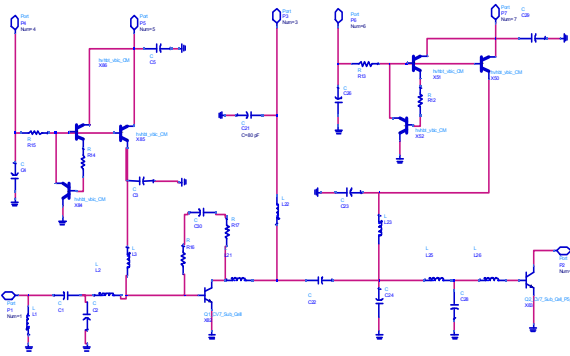


Fig. 2 Schematic of two stage TriPower MMIC

From the device point of view, the finger layout, the ballasting resistance, and the Epi layer structure design also affect the HBT's linearity. While some of these parameters can not be arbitrarily changed without seriously affecting the device's performance and stability, it is possible, however, using a dynamical biasing scheme to improve the linearity under large signal operations. It is known that one of the main sources for nonlinearity of an HBT is the nonlinear turn-on, or the exponential I-V of the device. Under class AB operations, large signal swings encompass a large portion of this

nonlinear I-V, and therefore, causing significant distortion in the output. One way to alleviate this effect is to utilize a dynamic bias scheme, which is capable of sensing the input power and dynamically adjusting the (base) bias voltage. As the input power increases, the device is automatically biased to a higher  $V_{be}$  value thus avoiding the large impact from the nonlinear turn-on of the device. This sensing device for the input power can be easily implemented with a diode and a capacitor together with the current mirror bias circuit [12].

#### IV. EVALUATION BOARD DESIGN

The evaluation board uses Rogers 3203 material. The dielectric constant of the PCB is 3.02 and the board thickness is 20mils. Fig. 3 shows the schematic of evaluation board.

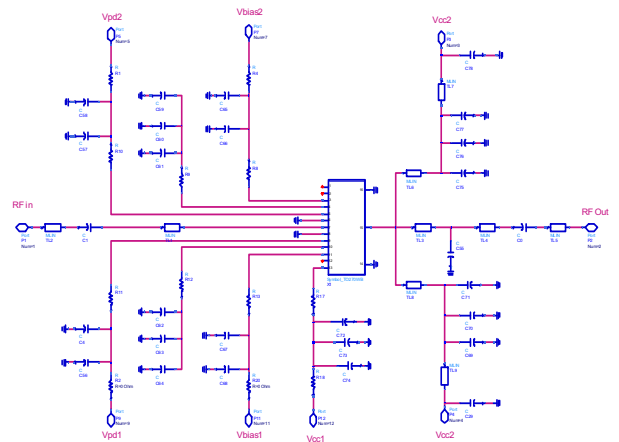


Fig. 3 Schematic of two stage TriPower MMIC

#### V. RF PERFORMANCE

##### A. Small Signal RF Performance

This 50W HVHBT MMIC's small signal gain and return loss are shown in Fig. 4. The devices were biased at 28V with a quiescent current of 320mA. The input return loss is below -18dB for frequency band between 750MHz and 960MHz. Its output is narrow band matched to target at the center frequency of 880MHz. Gain is around 30dB and gain flatness is around 2.2dB over the band.

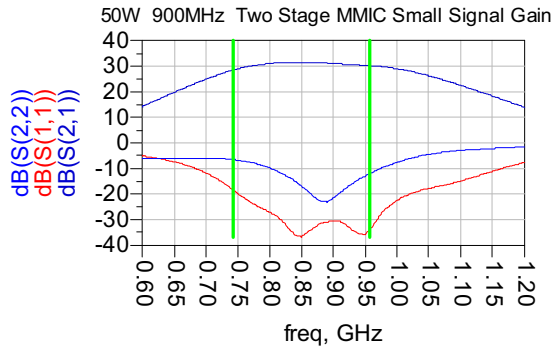


Fig. 4 50W HVHBT MMIC small signal RF performance

### B. Gain and Efficiency vs. Pout

The gain and efficiency of power sweep characteristics for our devices are shown in Fig. 5. The devices were biased at 28V with a quiescent current of 320mA. The three sets of curves correspond to results measured at 750, 880 and 960 MHz. Unlike those of typical LDMOS devices, the gain of our devices is quite flat over power all the way to near saturation and the  $P_{-1dB}$  point is close to that of  $P_{sat}$ . The measured  $P_{-1dB}$  is greater than 47dBm (more than 50W) with a collector efficiency of around 65%.

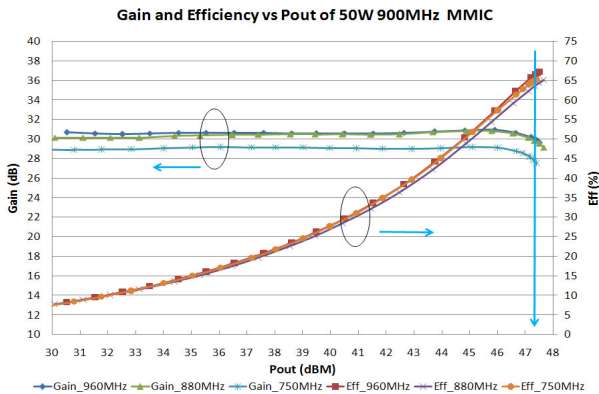


Fig. 5 Gain and efficiency vs. Pout over 750MHz—960MHz band

### C. Linearity Characterization

When subject to WCDMA modulation signals, the devices were tested for linearity. The linearity test results is shown in Fig. 6.

Testing with a Texas Instrument DPD system, this two stage MMIC has a very good linearity. The ACPR's before DPD correction were around -30dBc. With DPD correction, it can reach ACPR of -57dBc at  $P_{out}=41$ dBm with a collector efficiency of 36%. This is equivalent to >25dBc ACPR correction from DPD.

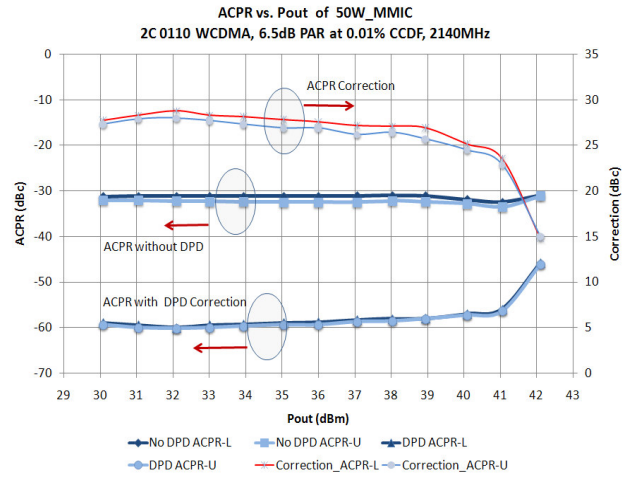


Fig. 6 ACPR with and without DPD correction

Testing with a low cost single die Scintera RF Pre-distortion system shown in Fig. 7, this two stage HVHBT MMIC also shows a reasonable linearity as shown in Fig. 8. Its ACPR can reach <-55dBc at  $P_{out}=37.5$ dBm. This is close to 22dBc correction in ACPR. This provides a very low cost and a very easy to use linearization scheme.

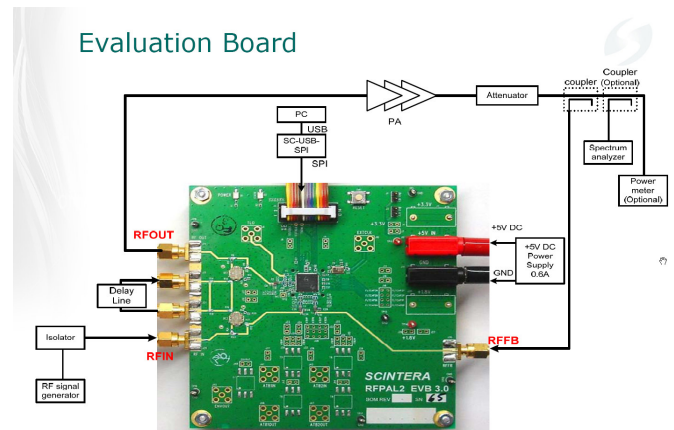


Fig. 7 Scintera RF Pre-distortion system board

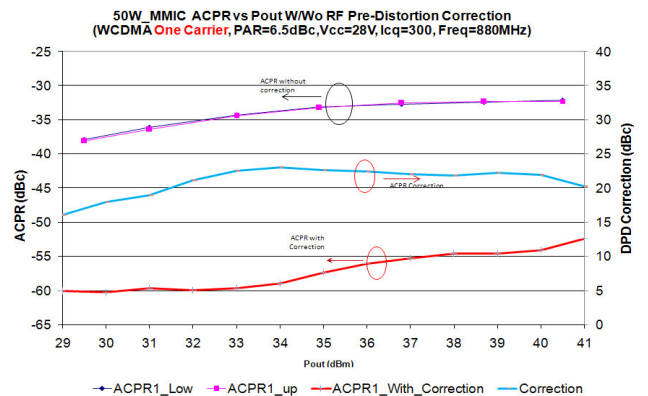


Fig. 8 RF Pre-distortion correction by Scintera system

#### D. RF Performance over Temperature

With a temperature compensated current mirror bias circuitry, this 50W MMIC has a very good temperature characteristics over a wide temperature range. Fig. 9 shows the measured gain and efficiency over output power at 85C, 25C and -40C. There is an around 5.5dB change in gain and less than 5% change in the quiescent current over this temperature range.

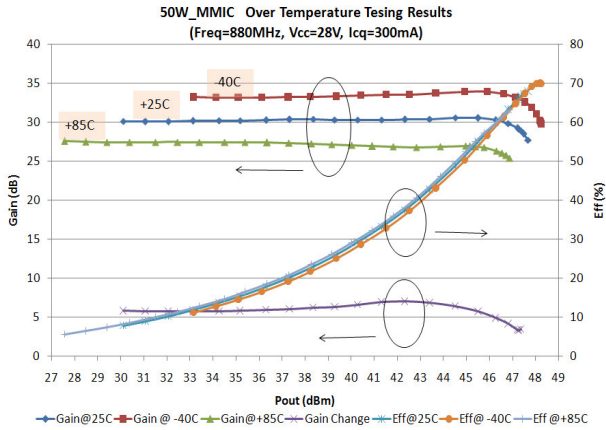


Fig. 9 Gain and efficiency of 50W MMIC over temperature

#### VI. RF OVER DRIVE TEST

We have performed RF overdrive test to evaluate the ruggedness of this MMIC die. The test data are shown in Fig. 10. An input over-drive of 10dB beyond P1dB point was observed without any device damage.

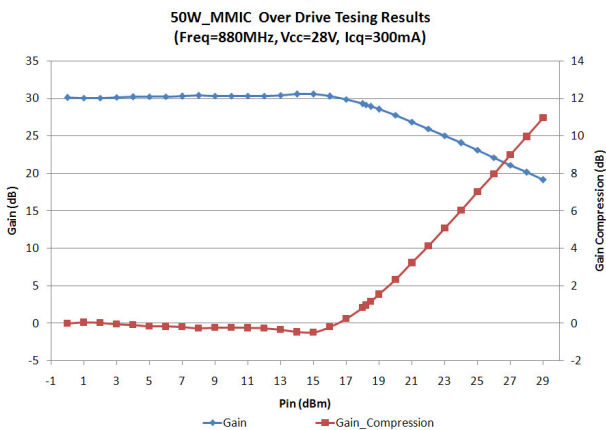


Fig. 10 880MHz TriPower MMIC over drive test

#### VII. CONCLUSION

We have demonstrated for the first time to our knowledge a single chip 50W InGaP/GaAs HVHBT MMIC with an excellent RF performance for base station applications. For

750-960MHz band, this new MMIC can deliver 47dBm, or 50W, at P-1dB with a collector efficiency of 65% and a gain of 31dB. Under a WCDMA two carriers signal with a DPD correction, it is able to deliver 41dBm (12.5W) output power with an ACPR of -57dBc and a collector efficiency of 36%. This high power, high efficiency performance achieved with a DPD circuitry provides a very promising solution for future green base station power amplifier design. The combination of a high power, a high efficiency, and a high linearity with DPD correction, InGaP/GaAs HVHBT technology has once again demonstrated its advantages in nature to become an excellent choice for the future linear power amplifiers in the infrastructure market.

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