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Analysis of The Unbalanced Feeding Effect on Discrete Device with Large Die Size

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***Abstract*—This paper focuses on analyzing the unbalanced feeding effect on RF power transistors, which can be generated from the input and output transition structures when they are connected to a relatively large size die. Such an effect can cause degradation of device's RF performance. A TGF2023-10 transistor assembled inside a PowerBand^{TM} package is used as an example to illustrate the effect. By modeling the input and output transition structures as one-port to multi-port transition networks, parameters based on the total difference of the transmission and reflection coefficients on the multi-port side are defined to quantify the unbalanced feeding effect.**

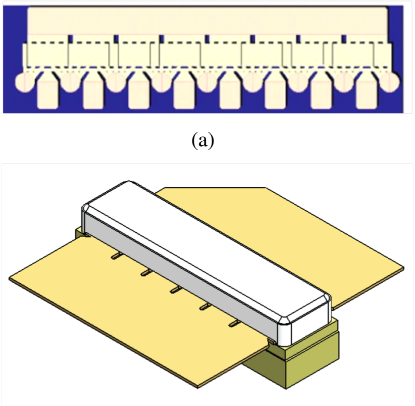
***Index Terms*—Discrete device, Gallium Nitride, power scaling and unbalanced feeding effect**

I. INTRODUCTION

Discrete field effect transistors (FETs) offer a relatively easier and lower cost solution for RF and microwave power amplifier design and implementation. For high power applications, discrete FETs are built with large gate periphery dies which have a multi-finger structure. Multiple fingers on the same die can cause RF performance degradation through non-uniform thermal distribution [1] and electromagnetic (EM) inductance, propagation and phase delay effects [2]. However, these are not the only reasons for effective power density reduction of large size discrete transistors. This paper will show that, with increasing frequency of operation, the unbalanced feeding effect generated from the input and output transition structures connected to the transistor can cause degradation of device's RF performance as well.

As a developing technology, GaN-based transistors exhibit substantial advantages over devices based upon other materials (such as GaAs or InP) having higher power density and higher power added efficiency (PAE). Based on both simulation and measurement results, a GaN-on-SiC transistor is used in the paper as an example to illustrate the unbalanced feeding effect. The higher power density allows GaN-based devices to have smaller gate periphery for applications with the same output power level, which reduces performance degradation from die size scaling. These smaller periphery die are being typically used with packages developed for lower power density semiconductors such as silicon LDMOS. This leads to a significant physical dimension mismatch between the package lead width and the GaN die width. This investigation proposes that this dimensional step change makes unbalanced feeding effect become more dominant.

Besides describing such an effect through both simulation and measurement, the paper also presents analysis on the input and output transition structures, where they are modeled as one-port to multi-port transition networks, and the total difference of the transmission and reflection coefficients on the multi-port side are used as parameters to quantify the unbalanced feeding effect.



(a)

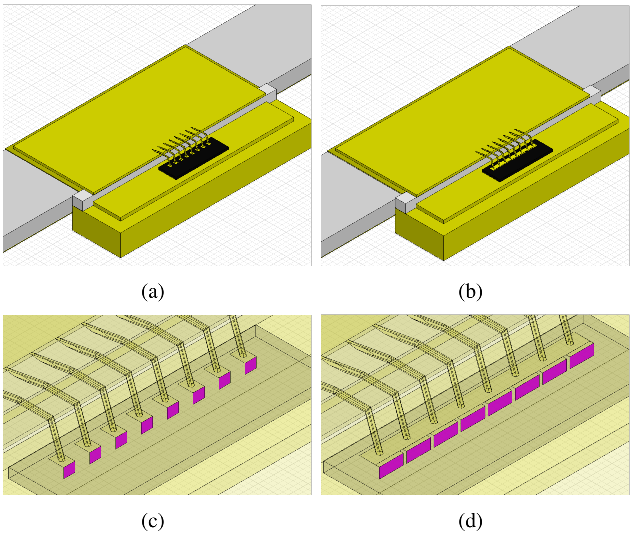
(b)

Fig. 1: (a) TGF2023-10 transistor and (b) PowerBand^{TM} package.

II. DEVICE MODELING AND PERFORMANCE CHARACTERIZATION

A TriQuint Semiconductor TGF2023-10 discrete GaN FETs [3] is used and assembled in a PowerBand^{TM} package [4], as shown in Fig. 1. The active device has 10 mm total gate length and is constructed based on eight 1.25 mm unit FET cells. It is placed at the center position inside the package, and connected to package leads with 2 mil diameter bond wires, where each wire length is kept to be minimum while satisfying the mechanical requirements.

Ansoft HFSS is used to model and simulate the input and output transition structures, which include device package, bond wires and bonding pads on the die, as shown in Fig. 2(a) and (b). A short section of 8.5 mm wide microstrip line on 25 mil Rogers RO3210 substrate is placed under the package leads to model the transition from the fixture, describing the fixture board material used in the load-pull measurement. A wave port is defined at the beginning of the microstrip line as the excitation. Eight lumped ports are used as terminations at the end of the bond pads, where the port size matches with the pad width and die thickness, as shown in 2(c) and (d). The whole structure is modeled as a one-port to eight-port



(a) (b) (c) (d)

Fig. 2: Input (a) and output (b) feeding structure models. Lumped port setup for the input (c) and output (d) feeding structures.

transition network, which allows us to analyze how each unit cell of the transistor is fed and terminated.

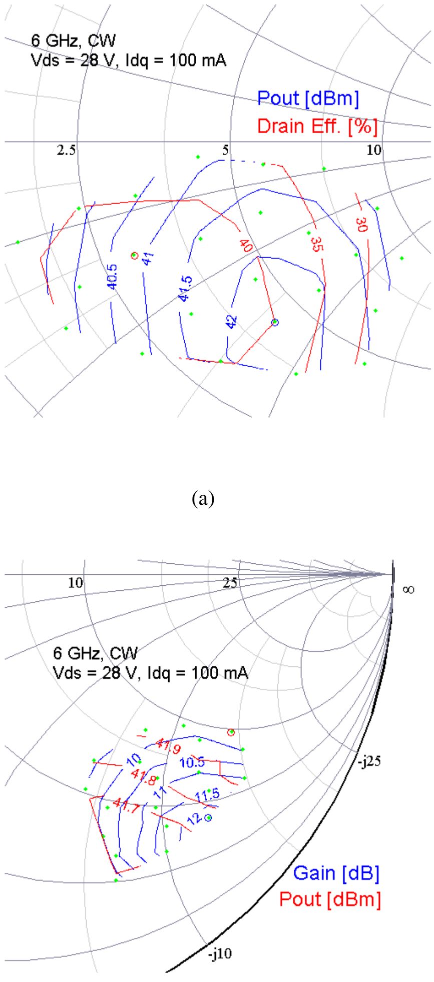
Utilizing the *probe based simulation technique* [5], based on a 16-port 28 V small signal S-parameter for TGF2023-10 transistor, it predicts that the packaged device can output 33.7 W of power with 54.6 % of drain efficiency at 6 GHz CW mode with 28 V drain bias. This is simulated by assuming that the transistor is fed uniformly and the input and output transition structures only introduce extra losses. If S-parameter blocks of the input and output feeding structures are included in the simulation, under the same operating conditions, the estimated device performance at the package reference plane has only 27.8 W output power associated with 46.3 % drain efficiency.

The packaged device is also measured and characterized with a standard load-pull setup at 6 GHz CW mode for a 28 V drain bias. By calibrating the setup to the device reference plane, the load-pull and source-pull data at 1 dB gain compression is measured and shown in Fig. 3. Based on the power sweep measurement at the optimum load and source impedances, as shown in Fig. 4, the device can output 43.7 dBm or 23.7 W of power at 3 dB gain compression with 43.4 % of drain efficiency.

TABLE I: Simulated and measured packaged device RF performances at saturation.

	P_{out} (W)	Drain Eff. (%)
Simulated w/o Unbalanced Feeding	33.7	54.6
Simulated w Unbalanced Feeding	27.8	46.3
Measured (at 3 dB compression)	23.7	43.4

The simulated and measured device saturated performances are summarized in Table I. The discrepancy between the data simulated with unbalanced feeding effect and the measurement might be due to the lack of thermal effect modeling across the transistor in the simulation. The data show that there is a $15 - 20\%$ performance degradation caused by input and output transition structures. Thermal scan images were also taken when the device is driven under saturation, as shown in



(a)

(b)

Fig. 3: Measured load pull (a) and source pull (b) contours at 1 dB gain compression at the device reference plane.

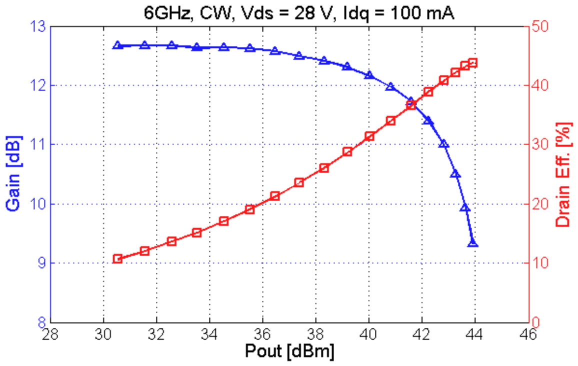
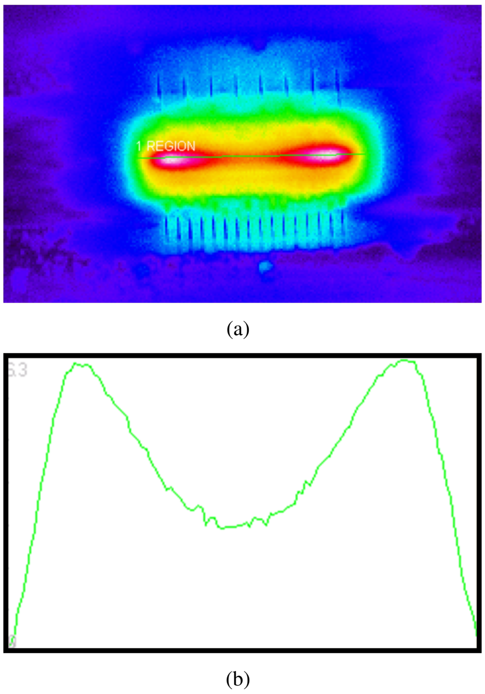


Fig. 4: Power sweep measurement at the device reference plane with optimum source and load impedances.



(a)

(b)

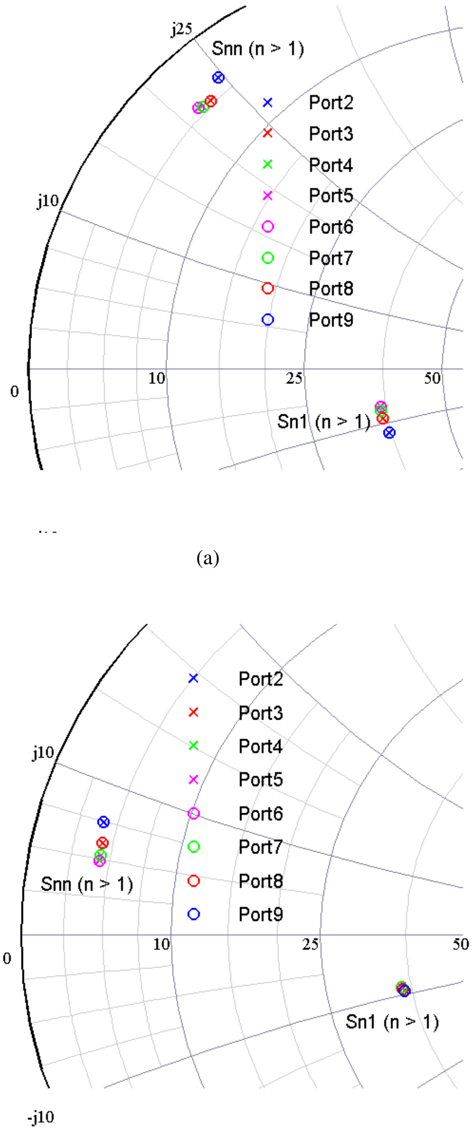
Fig. 5: Thermal image (a) of the transistor when it is driven into saturation and the corresponding thermal profile (b) across the center of the transistor.

Fig. 5. It is obvious that unit FET cells across the die are not performing uniformly, where the cells closer to the edges are driven harder and are dissipating more heat.

III. Analysis and Discussion

To better understand the phenomenon, the simulated 6 GHz $S(n,1)$ and $S(n,n)$ (for $n > 1$) responses of the input and output transition structure are plotted in Fig. 6, where $S(n,1)$ is defined as the through loss between the fixture port and any unit FET cell port, and $S(n,n)$ is defined as the reflection coefficient at any unit FET cell port. It can be seen that, with the current layout of the input and output bond pads and bond wire bonding profile, the transmission coefficients of the output structure are more similar for each unit cell than the ones of the input, where the reflection coefficients for both input and output are relatively spread out between cells.

The input transmission coefficients $S(n,1)$ represents how the input power is split and fed into each unit cell of the transistor, and the output transmission coefficients S(n,1) represents how the output power is combined. Ideally, all $S(n,1)$ of the input and output structures should be kept the same, respectively. This allows all the unit cells to be driven and combined uniformly. The input and output reflection coefficients $S(n,n)$ determines how each unit cell is terminated. It would be preferred to have the same $S(n,n)$ on the input and output, respectively, which lets all unit cells operate in the same way.



(a)

(b)

Fig. 6: Simulated S(n,1) and S(n,n) responses (for $n > 1$) for the input (a) and output (b) feeding structures.

In order to quantify the difference of transmission and reflection coefficients between unit cells, we define $\Delta S(n,1)_{\text{total}}$ and $\Delta S(n,n)_{\text{total}}$, where

$$\Delta S(n,1)_{\text{total}} = \sum_{i=2,j=i+1}^{i=8} mag\left(S(i,1) - S(j,1)\right), \quad (1)$$

$$\Delta S(n,n)_{\text{total}} = \sum_{i=2,j=i+1}^{i=8} mag\left(S(i,i) - S(j,j)\right). \quad (2)$$

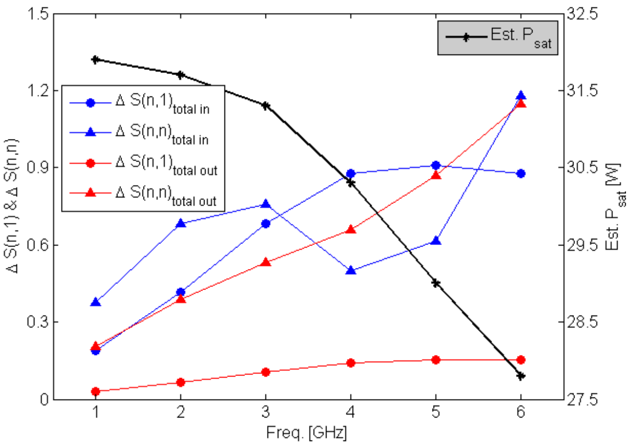


Fig. 7: Power sweep measurement at the device reference plane with optimum source and load impedances.

By using symmetry, Eq. (1) and (2) can be written as:

$$\Delta S(n,1)_{\text{total}} = 4 \cdot \sum_{i=2,j=i+1}^{i=4} mag\,(S(i,1) - S(j,1)), \tag{3}$$

$$\Delta S(n,n)_{\text{total}} = 4 \cdot \sum_{i=2,j=i+1}^{i=4} mag\,(S(i,i) - S(j,j)). \tag{4}$$

Figure 7 shows the calculated $\Delta S(n,1)_{\text{total}}$ and $\Delta S(n,n)_{\text{total}}$ for both input and output transition structures from 1 to 6 GHz with 1 GHz step size, associated with simulated saturation output power of the device across the same frequency band. It can be seen that as the value of $\Delta S(n,1)_{\text{total}}$ and $\Delta S(n,n)_{\text{total}}$ increases, the output power of the device decreases, which can also be translated as an increasing of the unbalanced feeding effect.

IV. CONCLUSION

In summary, through both simulation and measurement, the paper has illustrated that how the unbalanced feeding effect can cause RF performance degradation of a discrete device, where such an effect is generated from the input and output transition structures connected to the transistor. The analysis was done based on a discrete device built with TGF2023-10 transistor assembled in a PowerBand$^{\text{TM}}$ package. A 3D EM software, Ansoft HFSS, was used to simulate the electrical response of the transition structures, and they were modeled as one-port, input and output of the package leads, to multi-port, unit FET cells, transition networks. The total difference of the transmission and reflection coefficients, $\Delta S(n,1)_{\text{total}}$ and $\Delta S(n,n)_{\text{total}}$, on the multi-port side can be used as parameters to quantify the unbalanced feeding effect from the transition structures, where larger value of $\Delta S(n,1)_{\text{total}}$ and $\Delta S(n,n)_{\text{total}}$ translates to a higher unbalanced feeding effect and lower RF performance of the device.

ACKNOWLEDGMENT

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