A 40 GHz Power Amplifier Using a Low Cost High Volume 0.15 um Optical Lithography pHEMT Process

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***Abstract* — A 40 GHz power amplifier is realized with a new 0.15 um optical lithography pHEMT process developed for low-cost microwave and millimeter wave circuits. Several Ka and V Band market requirements have driven demand for higher bandwidth, low-cost, integrated circuits. A 40 GHz power amplifier is used to demonstrate the process capabilities, starting from the initial design phase and culminating with the fabrication and measurement of the solid state power amplifier.**

***Index Terms* — Microstrip components, millimeter wave power amplifier, pHEMT, impedance matching.**

I. Introduction

A 40 GHz power amplifier has been designed and fabricated using a 0.15 um optical lithography pseudomorphic high electron mobility transistor (pHEMT). The high volume 150 mm process named TQP15, has been developed by TriQuint Semiconductor to meet increased demand for microwave and millimeter wave integrated circuits with good power performance at higher frequencies. The amplifier has been designed for 15 dB of gain and 28 dBm of output power from a 3 V power supply. Related market applications include Automotive Radar, Point-to-Point Radio, VSAT, and other Ka and V band applications. Several papers have reported amplifier performance in the Ka and Q bands, [1] – [8], but these amplifiers use direct write e-beam gates and air-bridge interconnect, technologies less suitable for high volume low cost manufacturing.

The simulation, fabrication and measurement of the amplifier demonstrate the process capability. DC and RF measurements and load pull data, tuned for power, illustrating the gain and power added efficiency (PAE) are presented.

A description of the design and performance of the 3-stage power amplifier (PA) is presented. Transistor cell DC and RF characteristics, impedance transformations and matching networks are described.

II. Process and model Overview

The TriQuint TQP15 process is a refractory gate technology that is fabricated on 150 mm diameter 100 um thick GaAs wafers with substrate via holes. TQP15 is an extension of the work performed to develop the TQP25 [9] and TQP13 [10] process technologies. These processes use I-line steppers and sidewall spacer gate construction for high throughput and low-cost manufacturing.

A summary of the process parameters is presented in Table I.

TABLE I

TQP15 Process Summary

Process Specifications, Vds = 3.0 V		
Parameter	**Typical Value**	**Units**
Lg	0.15	um
Vp	-1.0	V
BV min/typ	12/14	V
Imax/Idss	550 / 310	mA/mm
Gm	450 @ Idss	mS/mm
Ft / Fmax	65 / 125 @ Idss	GHz
Process Passive Elements		
Parameter	**Typical Value**	**Units**
Resistors	50 / 225	Ω/sq
BLMET (0.62um)	50	mΩ/sq
Met 2 (4um)	6	mΩ/sq
MIM Cap	0.62	fF/um^2

The TQP15 optical gate technology enables a less expensive solution for the design space. The refractory gate enhances the thermal stability and the long term reliability of the transistor. A scanning electron microscopy image of the gate structure is shown in figure 1.

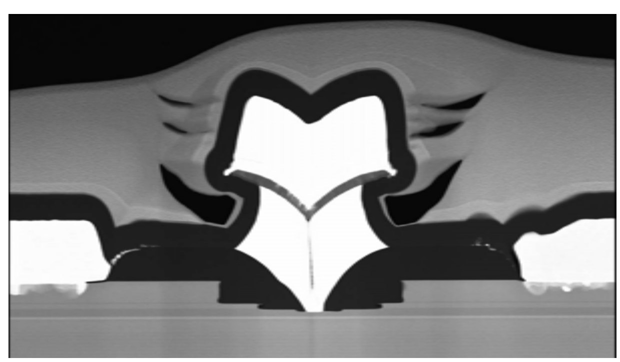

Fig. 1. Cross-Section Image of Gate

The planarized benzocyclobutene (BCB) interlayer dielectric provides more uniform electrical performance for different packaging conditions, as compared to the more typical air-bridge process. A pictorial of the process cross section, with active and passive components, is shown in figure 2.

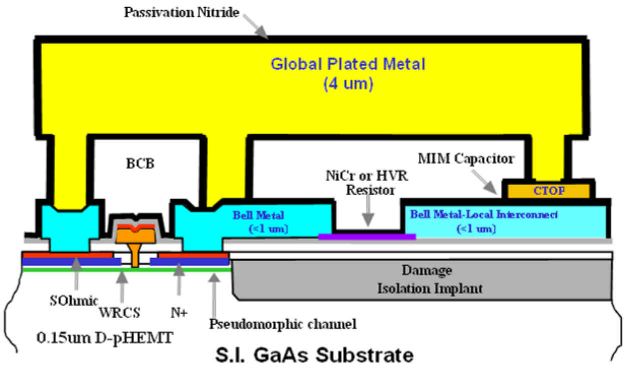

Fig. 2. Process Cross-Section of TQP15

Initial device characterization and models were derived from the coplanar waveguide (CPW) ground-signal-ground (GSG) test configuration shown in figure 3.

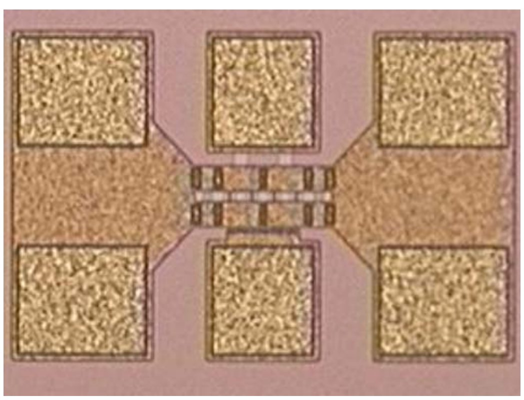

Fig. 3. 4 x 50 FET in a CPW Test Structure

Further characterization and modeling were derived from test configurations using substrate via holes and microstrip launches. Associated on-wafer LRM calibration structures were included. Figure 4 shows a ten finger device with a gate width of 60 um.

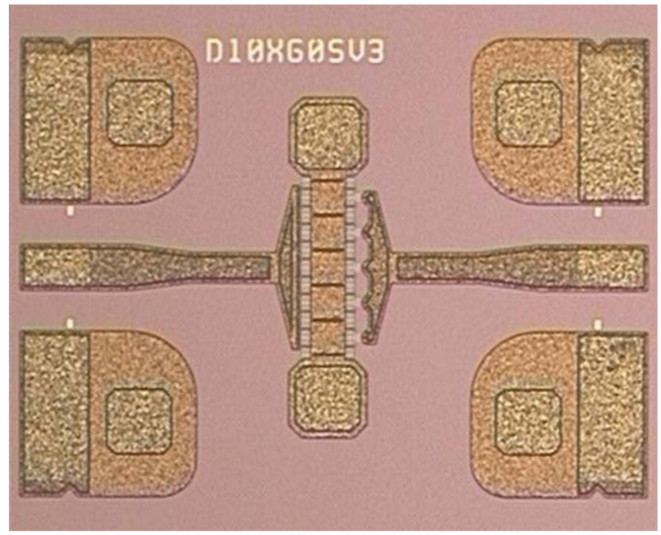

Fig. 4. 10 x 60 FET in Microstrip GSG Test Structure

III. Design Methodology

The PA was designed using the TQP15 Process Design Kit (PDK) with a commercially available harmonic balance simulator. The TOM4 pHEMT model was extracted from DC and multiple bias S-parameter measurements. The resulting component model accuracy improves agreement between simulation and measurement of the fabricated amplifier.

A microstrip line approach was selected in place of CPW to avoid excessive metallization and potential transmission line modeling problems.

The output stage was designed to deliver over 28 dBm of output power from eight unit cells of 10 x 80 um each. The driver and second stage use 10 x 60 um cells for appropriate gain and output power. The gate periphery ratio of stages 1, 2, and 3 is 1:2:2.75. The die size is 3.1 mm by 3.1 mm, driven primarily by the size of the third stage transistor. A picture of the die is shown in figure 5.

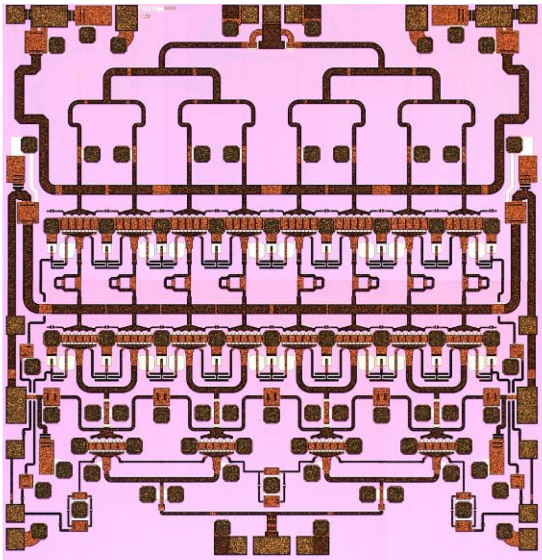

Fig. 5. Power Amplifier MMIC

A larger output current is required to generate the required 28 dBm of output power from the relatively low supply voltage of 3 V. In addition to the device size, the larger output current requirement results in low output impedance for the third stage transistor which must be impedance matched to a 50 Ohm system impedance. Microstrip transmission lines were designed to provide the proper impedance transformation between stages and for the specified 50 Ohm input and output impedances.

The DC drain supply current feed is integrated into the output matching circuit which requires the microstrip transmission lines to be sized appropriately for the DC current as well as the impedance transformation. The biasing network is symmetrically fed to minimize phase differences. The matching and DC feed networks employ MIM capacitors and thin film resistors in addition to the microstrip transmission lines.

The thin film resistors are used to suppress and prevent in-band and odd mode oscillations, especially in power combing configurations as described in [2],[3], and [7]. The resistive elements are used in series between the parallel drains in the output cell.

A low voltage high power design at high frequencies is complicated by the steep load line restrictions and the low impedance required for obtaining the required output power. The gate voltage is set to hold a predetermined drain current for power efficient deep class AB operation. Power efficient operation, matching circuit, and bandwidth limitations are more thoroughly addressed in [4].

IV. Measurements

Two test transistors were used to compare simulated performance to measured performance. The simulated versus measured results are shown here. The simulated and measured performance of the complete three stage 40 GHz amplifier will be shown in the oral presentation of this paper.

The DC I-V characteristics of the 4 x 40 um pHEMT are simulated using the TOM4 model and compared to the measured characteristics. The results are shown in figure 6. Measurements were taken on a process nominal full thickness wafer at room temperature.

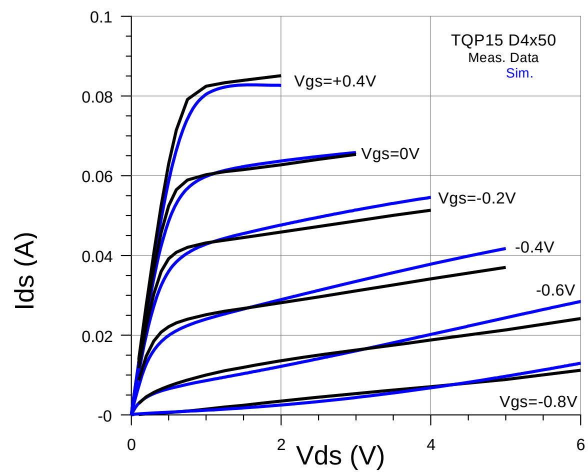

Fig. 6. IV Curves for the 4 x 50 Depletion Mode pHEMT FET

Simulated and measured transconductance and drain current versus gate voltages (-1.2 V to +0.8 V) are shown in figure 7.

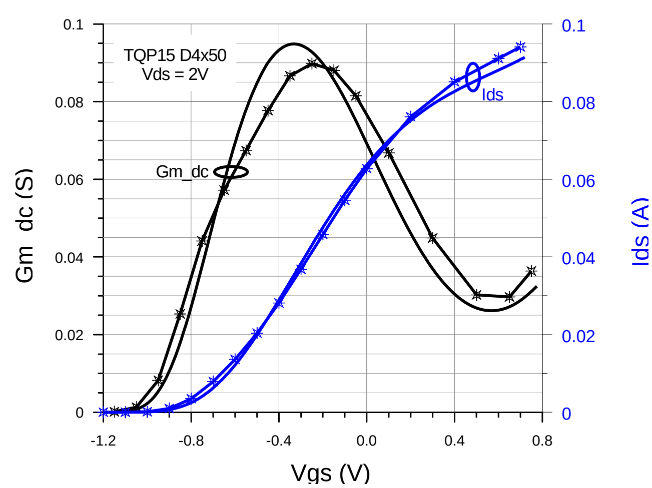

Fig. 7. DC Drain Current and Transconductance at Vds=2V (measured data marked with symbols)

S-Parameter measurements for three volt operation through 50 GHz are shown in figure 8.

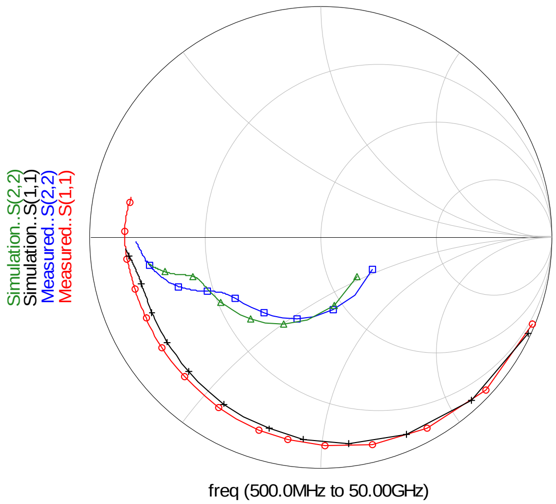

Fig. 8. S11 (Circles) and S22 (Squares) are Measured Data and S11 (Crosses) and S22 (Triangles) are Model Simulations

Additional S-parameter measurements were made using 100 um thick wafers with substrate via holes at the ground pads and at the pHEMT source (figure 4). The Maximum Available Gain (MSG) from 500 MHz to 50 GHz is shown in Figure 9. The MSG/MAG transition is above 30 GHz, with the substrate via holes in the ground path.

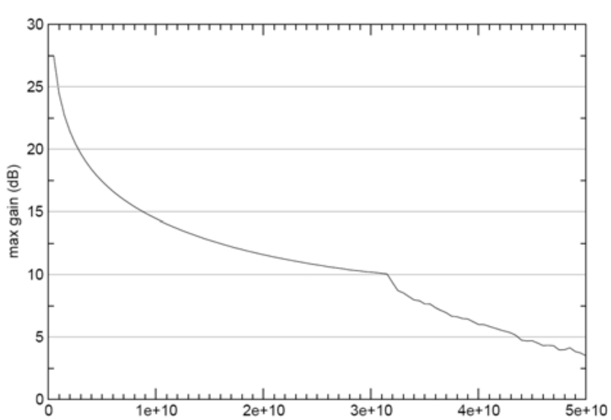

Fig. 9. Maximum Gain Plot to 50 GHz

Load pull data has been measured. Figure 10 shows the gain and Power Added Efficiency (PAE) performance at 21 GHz.

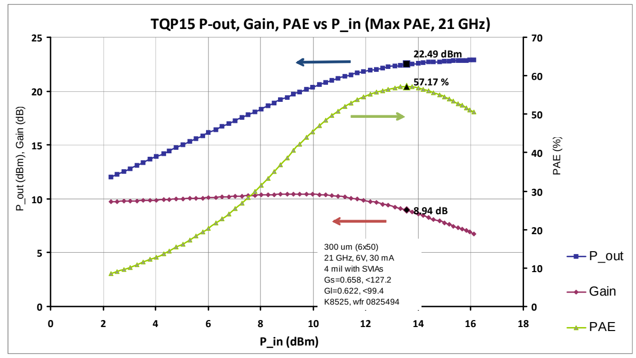

Fig. 10. TQP15 6x50 um Device Load Pull Data at Maximum Power Tune, 21 GHz, Vdd = 6 Volts and Ids = 30 mA

The amplifier die, bypass capacitors and probe pads were attached to a gold flashed carrier. The amplifier, mounted on the test carrier was tested using a wafer probe station with GSG probes for the RF signals and DC probe needles for the DC voltage supply. A picture of the die on its test carrier assembly is shown in figure 11.

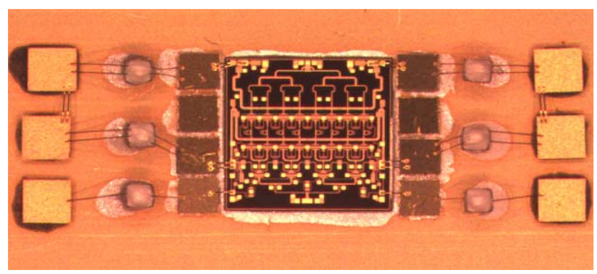

Fig. 11. Amplifier Die, Epoxy Die Attached to a Gold Flashed Carrier with Wire Bonded Bypass Capacitors and Probe Pads

The test setup at this writing is unable to provide enough RF drive to compress the amplifier. The test setup will be modified to provide measured data in time for the oral presentation of this paper. Figure 12 shows the simulated gain, output power, and PAE versus input power.

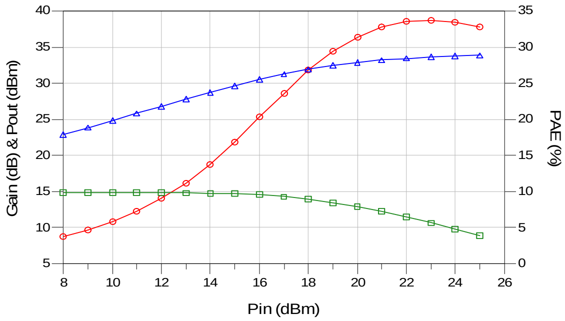

Fig. 12. Simulated Gain (Squares), PAE (Circles), and Pout (Triangles) for the 3 Stage Amplifier

V. SUMMARY

This work describes a three stage 40 GHz power amplifier design using the TQP15 0.15 um high volume optical lithography pHEMT process. The work presented in this paper was used as a vehicle to provide information for PA applications at 40 GHz and to demonstrate the ability to design and fabricate a PA through a standard design flow using a low-cost high-volume manufacturing process.

A 28 dBm output power amplifier operating at 3 volts with a small signal gain of over 15 dB has been demonstrated. Simulated and measured performance of the circuit components has been shown. Simulated and measured performance of the complete three stage amplifiers will be shown in the oral presentation. Future work includes the investigation of performance improvement from slotted substrate via holes directly under the source contacts, and integrated active bias networks.

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