APPLICATION NOTES: Designing High Efficiency Applifiers using HFETs

HFET

INTRODUCTION

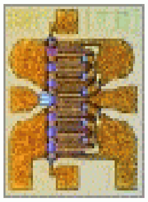
TriQuint Semiconductor has developed a range of Heterostructure FETs designed for power amplifier applications where high power-added efficiency is a key specification. They also offer the unique possibility to construct amplifiers with high efficiency and low intermodulation products near compression. This technical note describes how power amplifiers may be designed using this device, and includes a specific design example. The reader is referred to Ref 1 and Ref 2, which describe the structure and properties of the device and contain measured data from a number of HFET power amplifiers. Copies of Ref 2 are available from TQS Microwave GaAs Products (MGP) on request.

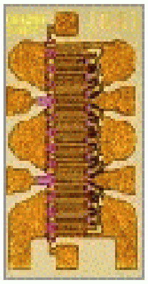
The TQS HFET family consists of four devices with different gate peripheries (see below). One gate and one drain pad are provided per 1.2 mm of gate periphery for each device with gates to the left and drains to the right. Sources are connected to the backside of the chip using via holes. Extra gate and in some cases elongated drain pads are provided to allow devices, connected in parallel to achieve higher power levels, to be interlinked to avoid odd-mode oscillations.

Devices should be soldered to the baseplate using Au/Sn eutectic. It is recommended not to exceed 300 deg C for greater than three minutes during soldering. For experimental purposes only, epoxy mounting has been used. The use of epoxy will result in slightly degraded performance due to the higher device operating temperature. This will also have a negative effect on device lifetime, of course.

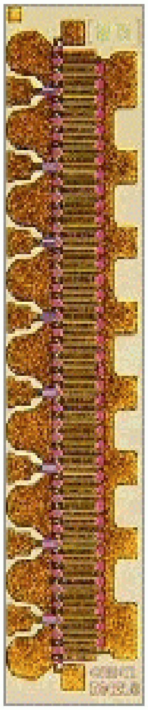
DESCRETE HFETS

TGF4230: 1.2 mm, 0.572 x 0.699 mm (0.023 x 0.028 in.)
TGF4240: 2.4 mm, 0.572 x 0.978 mm (0.023 x 0.039 in.)
TGF4250: 4.8 mm, 0.572 x 1.334 mm (0.023 x 0.053 in.)
TGF4260: 9.6 mm, 0.572 x 2.324 mm (0.023 x 0.092 in.)


TGA4230


TGA4240


TGA4250


TGA4260

SPECIFICATION

8.5 GHz V_{DS} = 9 V

TYPICAL DC CHARACTERISTICS

PARAMETER		NOMINAL	UNIT
G_M	Transconductance	165	mS/mm
I_{DSS}	Drain Saturation Current	245	mA/mm
I_{MAX}	Maximum Drain Current	490	mA/mm
V_P	Pinch Off Voltage	-1.85	V
BV_{GS}	Breakdown Voltage Gate-Source	-22	V
BV_{GD}	Breakdown Voltage Gate-Drain	-22	V

DEVICE SELECTION AND CHARACTERIZATION

The “Specifications” section gives an indication of what size device is required to meet a given power specification. The power and efficiency figures are those obtained with a load impedance chosen to be a compromise between power and efficiency. It is possible to achieve slightly higher power levels with a lower load impedance (with lower efficiency), and higher efficiencies with a higher load impedance (with lower power). Determining the optimum load impedance for a particular application is often best achieved experimentally by designing and tuning a test amplifier, using the compromise load impedance discussed herein as a starting point. Load-pull, particularly with the larger devices, is of limited value, since the desired impedance transforms are large and difficult to achieve with normal tuners with low loss. In some cases, prematching can be useful, where lumped components are mounted close to the device to perform some degree of impedance transformation to ease the task of the tuners.

BIAS POINT

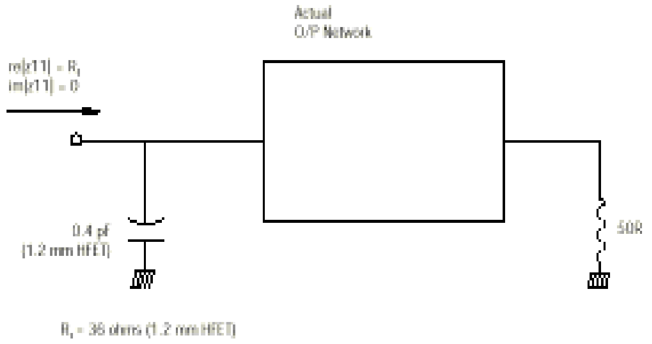
The HFET structure is designed to operate in Class AB for high efficiency applications. The choice of the quiescent DC bias point depends on the application, but in general is in the range 0.05 to 0.25 IDSS. Over this range of quiescent currents, the gain generally varies by less than 1-dB for a single stage amplifier, and for single tone applications, the exact bias point is relatively uncritical. Where intermodulation performance is important, however, the bias point needs to be set carefully, as it has a large effect on the level of the intermodulation products.

OPTIMUM LOAD IMPEDANCE

In designing high efficiency amplifiers, the next item to consider after the bias point, is the optimum load impedance at the fundamental frequency. Extensive load-pull measurements have shown that the optimum efficiency load for a 1.2 mm HFET is 64 ohms resistive, when the output capacitance is embedded into the output network. For maximum power the optimum load falls to about 36 ohms. These loads have been found experimentally to scale linearly with device periphery, making amplifier design with larger devices relatively straightforward. Further experimental work on a number of L/S Band amplifiers has also demonstrated that an optimum load (short circuit) at the second harmonic can improve the efficiency by up to 6 percentage points. For narrow-band amplifiers the short at the second harmonic can be implemented by a simple shorted stub (at the fundamental). This method works well with any output network topology provided the stub can be located close enough to the device so that the drain bondwires do not affect the impedance to any great extent. A second method, which applies mainly to low-pass networks, is to optimize the output circuit simultaneously to present the correct load at the fundamental and a short at the second harmonic. With large-periphery or paralled devices this is often the only method that can be used, as the layout will usually not permit any other implementation.

While non-linear models are being developed and verified, most amplifier designs in-house are using the above load pull data to set the output load impedance target. For a 1.2 mm device, the optimum power load is represented by a parallel RC network, where R = 36 ohms and C = 0.4 pF. The design of the output network is much simplified if the capacitive element is "absorbed" into the output network, as shown below, leaving the optimizer to search for a simple resistive load. As preveously noted, these elements scale with device size, so for a 9.6 mm device, the optimum load resistance for power would be 4.5 ohms, with a 3.2pF shunt capacitor embedded into the output network file as the first element. This design method is used in the example in Appendix 1.

RECOMMENDED METHOD FOR REPRESENTING LOAD IMPEDANCE



OUTPUT NETWORK DESIGN

Given the target load resistance, the output network may then be designed. Classical synthesis methods are applicable particularly for broad band designs, while simple Smith Chart methods may be used for narrow-band applications. A linear simulator may be used to optimize the circuit, for the desired load resistance over the band of interest. The reactive part should be kept to less than about 10% of the magnitude of the real part, ie., less than 0.45 ohms for a 9.6 mm output network. After the network has been optimized, it is often useful to check, using a Smith Chart, that the path chosen by the optimizer still makes sense, ie., there are no instances of networks following unnecessary paths (which will likely result in increased losses). Load line analysis techniques may be used to predict the power which will be delivered into the predicted load, if desired.

Another factor which needs to be considered in the design of the output network is the effect of losses. Since in general the output network is required to perform a large impedance transform, losses in the elements need to be minimized. Steps can be taken at the design stage to achieve this, by choosing optimum circuit topologies and constraining element values. Circuits which require large value series inductors or large value shunt capacitors tend to be more lossy, and should be avoided. Care needs to be taken when realizing the network also, by choosing low-loss components, especially shunt capacitors. In our experience, capacitors from different vendors have significantly different ESR values, and it is frequently worth the investment to characterize parts before using them (see Appendix 2). DC losses may be of significance also, especially in the drain bias circuit, and bias components should be constructed carefully to have a low DC resistance, as well as low RF loss.

INPUT NETWORK DESIGN

The input network of a high-efficiency amplifier has a dual role. It needs to provide the impedance match to the input of the device, as well as ensuring stability. A small signal model of a 1.2 mm HFET is included in the design example (Appendix 1) to allow the small signal performance of amplifiers to be simulated. In practice, it has been observed that the input VSWR of HFET amplifiers changes little as the device is driven into large signal conditions, validating a small-signal design approach for the input network.

The majority of HFET amplifiers designed at TriQuint Semiconductor have used low-pass input networks, with series and shunt resistive stabilization. The series stabilization can be realized as a resistor close to the FET gate, especially in low-frequency applications where some gain can often be given up in the interest of stability. For higher frequency applications the resistor may be partially bypassed, either with a simple capacitor or a resonant network. This allows the resistor to perform its stabilization function at low frequency without causing too much gain loss at the operating frequency.

If possible, the input network should present a short circuit to the device at the second harmonic, but frequently this is not possible due to the constraints of maintaining a good input match and stability. Losses in the input network also need to be considered, as it is very easy to lose a significant amount of gain, especially in shunt tuning capacitors. Frequently the design of the input network is more challenging than the output.

INTERMODULATION PERFORMANCE OF CLASS AB HFET AMPLIFIERS

The TQS HFET is particularly suited to applications where high efficiency and good intermodulation performance are needed simultaneously. This requires the device to be operated at a quiescent bias point quite close to pinchoff, where the intermodulation products are observed to reduce in level. This so-called "sweet spot" has been observed from L thru X-Band, and appears to be stable with temperature. When operated at the sweet spot, it can be seen that the IM products do not fall off at the "normal" rate, and in fact, stay at a relatively constant level over a 10 to 15-dB range of input power. The gate voltage required to achieve the sweet spot has been measured for a number of devices and does not seem to change significantly across a wafer, allowing larger amplifiers to be constructed using many devices in parallel. The largest gate periphery yet combined in a single-ended amplifier is 48 mm, and this amplifier still exhibited good sweet spot operation.

The HFET is also suited to multi-carrier applications where high peak power and good efficiency are required simultaneously. HFET amplifiers have been tested using the NPR method, in which the device is driven with a band-limited noise signal, to simulate the effect of multiple carriers. A narrow-band "notch" is generated in the center of the noise signal, by a suitable filter, and any intermodulation is observed as a reduction in the depth of the notch.

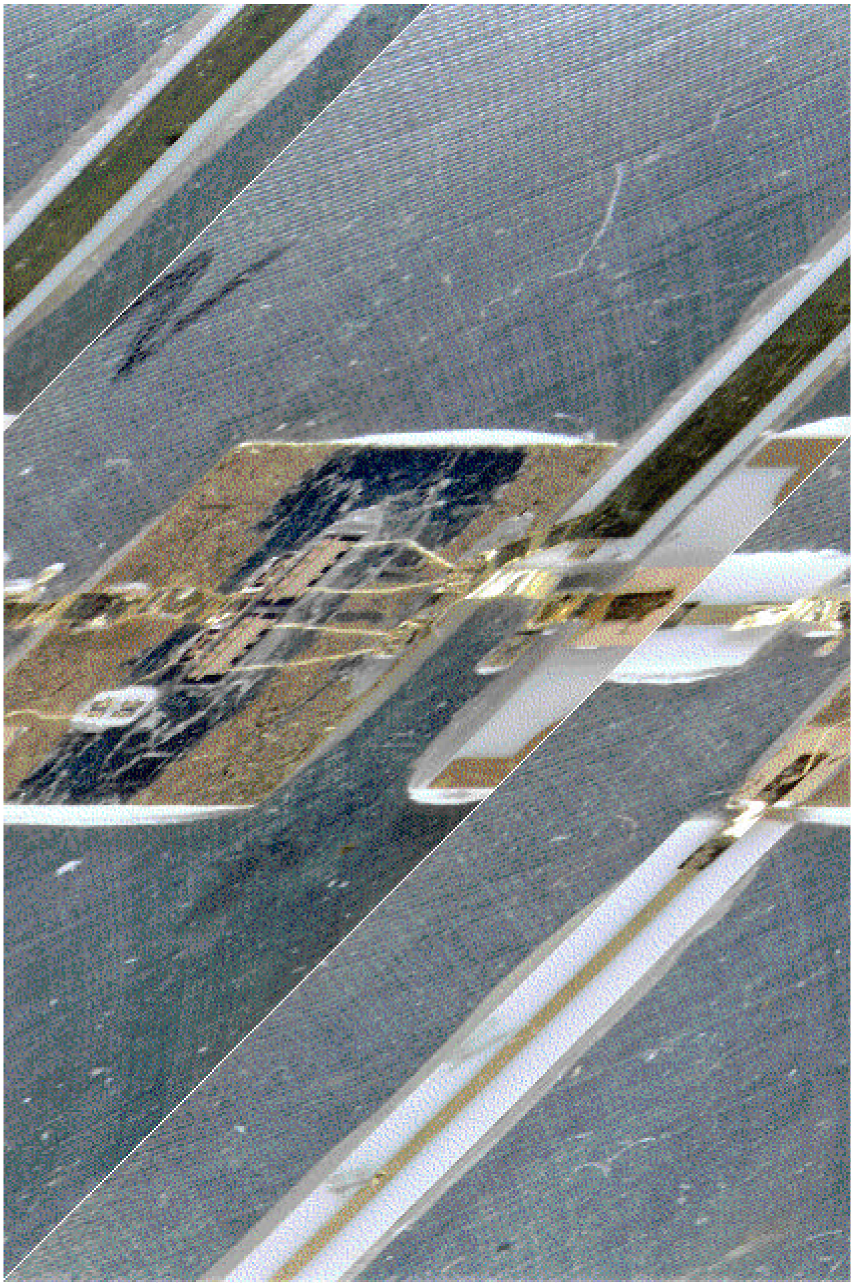
HYBRID IMPLEMENTATION OF HFET AMPLIFIERS

It is worth bearing in mind from the outset that prototype amplifers will almost certainly require some degree of tuning to achieve the desired performance. This is not believed to be associated with the design approach, but more with the way the elements are realized in practice in a hybrid circuit. Thus building-in ease of tuning should be considered when designing and laying out an amplifier. One key area here is in the design of inductors. In our experience, most tuning time is spent adjusting inductors. Often elements are rather critical, as it is notoriously difficult to predict the inductance of multiple wire-bonds (as used to connect to the gate and drain pads) to the required degree of accuracy. Bondwire sets can be tuned by adding or removing wires, adjusting their spacing or height above the groundplane. If wires are being removed to increase inductance, care should be taken not to exceed current handling ratings for the bondwires. With amplifiers using paralled devices, symmetry should always be maintained during tuning to avoid unequal power sharing across the devices.

Inductors using gold ribbons may be used to realise easily-tuned inductors, with high Q. The inductance of a ribbon is at a maximum when it loops up to the highest possible extent above the groundplane and may be reduced to a minimum value by bending it to the shape of a letter M. The “Maximum and Minimum Inductance” chart on page 7 gives the approximate inductance limits of 20-mil-wide gold ribbon inductors. The length shown is the active length of the gold ribbon. The ribbon needs to be cut longer, to allow for welding to the other components. The data shown in the “Recommended Method for Representing Load Impedance” diagram on page 3 was taken at 1.5-GHz, using 0.025" thick alumina launch substrates separated by 0.120".

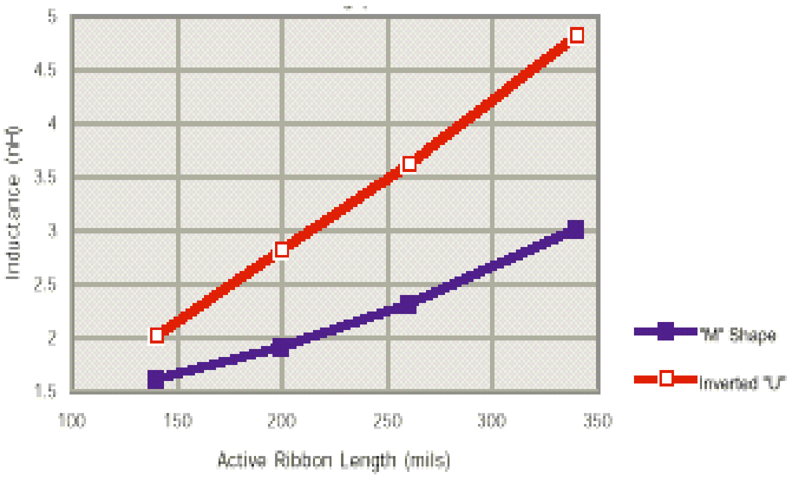
A photograph of part of an L-Band HFET amplifier is shown on page 6. This amplifier uses low pass matching circuitry for both input and output networks, shunt/series stabilizing networks in the gate circuitry, and a quarter-wave second harmonic trap in the output circuit. Gold ribbon inductors were used extensively. This amplifier achieved a power added efficiency in excess of 60% in L-Band.

LBAND HFET
HYBRID AMPLIFIER



MAXIMUM AND MINIMUM INDUCTANCE

20 mil Ribbon Inductor
Bringing 120 mil gap



MONOLITHIC IMPLEMENTATION OF HFET AMPLIFIERS

There are a number of reasons why the monolithic environment should be considered for higher power amplifiers. Firstly, it would eliminate the large number of bondwires used to connect multiple paralleled devices, with a consequent reduction in assembly cost and improvement in reliability. Also, it is quite difficult to control the length of the bondwires and their height above the groundplane, leading to variations in inductance in some production enviroments. Monolithic interconnections are more predictable and reproducible, as well as providing better controlled phase matching across the devices.

Another advantage of a monolithic implementation is the higher Q offered by MIM capacitors compared to wire-bondable ceramic capacitors, leading to lower circuit losses. The ability to incorporate resistors on-chip leads to easily implemented stabilization networks. Partial bypassing of series gate stabilization resistors is also possible, leading to increased in-band gain while maintaining low-frequency stability.

The design methodology used to develop a two stage MMIC power amplifier with 5 W output in X-Band is discussed in Ref 2.

References:

1. "High Linearity and Efficiency Power Amplifiers using GaAs Heterostructure FETs",
C. Suckling et al, Microwave Journal, April 1995 p258–262
2. "Heterostructure Devices and Applications",
TQS Technical Seminar Notes, MTT-S 1994

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!Example of 4.8mm HFET Power Amplifier. The amplifier was designed to characterise
!the TirQuint Semiconductor 4.8mm HFET (TGF4250) at 8.5 GHz. It consists of input and
!output matching substrates (0.005in Alumina), the HFET and a 1000pF decoupling
!capacitor and drain bias are fed through external bias tees.
!..........................................................................................................................................
DIM
LNG  MIL
FREQ  GHZ
CAP  PF
IND  NH
RES  OH
COND  /OH
TIME  PS
VAR
LI    #10  87        199  !length of input matching transmission line
WI  # 70  62                    130!width of input matching transmission line
W50=4.4  !width of 50 ohm line on input substrate
HI=5  !  thickness of input substrate
LO= 128 !length of input matching transmission line
WO=26  ! width of input matching transmission line
HO=5   !  thickness of output substrate
LBWI=.1  !    inductance of 4 1 mil bondwires 20 mils long (bent down for tuning)
LBWO=.07 !  inductance of 4 1 mil bondwires 12 mils long (bent down for tuning)
W51=4.4  !width of 50 ohm line on output substrate
!...........................................................................................................................................
EQN
LIR = 200 - LI
LOR = 200 - LO
!..........................................................................................................................................
CKT
!  4800 FET MODEL BLOCK
IND 1  2 L=.010525 ! Lg
RES 2  3 R=0.21075 ! Rg
SRC 3  5 R=.3025  C=4.84  !Ri,  Cgs
RES 3  5 R=20425 ! Rgs
VCCS 3  4  5  5  M=.5316  A=0  R1=1E19  R2=1E19  F=0  T=5.49 !gm,  A,  R1,  R2,  F,  Tau
CAP 3  4 C=.4015 !Cdg
RES  3  4 R=51000 !Rdg
CAP  4  5 C=1.013 !Cds
RES   4  5 R=24.5025 ! Rds
SRL  4  7 R=.165  L=.0055 ! Rd, Ld
SRL  5  0 R=.1  L=.011 ! Rs, Ls
DEF2P  1  7 MODEL3!4.8MMMODEL
!SHUNT STABILISING NETWORK  (ON INPUT SUBSTRATE) BLOCK
MSUB ER=9.85 H^HI T=.2 RHO=1 RGH=0
MLIN  1  2 W=1  L=6!bond wire
MSTEP  2  3 W1=1 W2=4  !step to bond pad
MLIN  3  4  W=4 L=4  !bond pad
MSTEP  4  5  W1=4  W2=1  !step bond pad to transmission line
MLIN  5  6  W=1  L=110  !transmission line
MSTEP  6  7 W1=1  W2=6  !step to resistor contact
MLIN  7  8  W=6  L=6  !resistor contact
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TFR  8  9  W=4  L=6 RS=20 F=0  !thin film resistor on substrate
MLIN  9  10 W=6  L=3  !half of bondpad
MLEF 10  W=6 L=3  !half of bondpad
IND  10  11  L=.3  !inductance of bondwire to external capacitor
CAP  11  0  C=1000  !external capacitor
DEF1P  1  SSTABG
!.................................................................................................................................
!INPUT NETWORK
MSUB ER=9.85 H=25 T=.2 RHO=1 RGH=0  !test fixture substrate
MLIN  1  2  W=22  L=250   !test fixture substrate
MSUB ER=9.85 H^HI T=.2 RHO=1 RGH=0  !matching substrate
MSTEP  2  22 W1=22 W2^W50  !step between 50 ohm lines on substrates
MLIN  22  3 W^W50 L ^LIR  !  length is (200 - LI) of 50 ohm line on matching substrate
MSTEP  3  33 W1^W50  W2^WI  !step 50 ohm line to matching element
MLIN  33  4 W^WI L^LI  !matching line
MSTEP  4  44 W1^WI  W2=30  !step to bondwires, W2 taken as width of set of gate bondwires
SSTABG  4  !shunt stabilisation network, see above
IND  44  5 L^LBWI  !gate bondwires
DEF2P  1  5 INPUT
!.................................................................................................................................
!OUTPUT NETWORK BLOCK
MSUB ER=9.85 H^HO T=.2 RHO=1 RGH=0  !MATCHING SUBSTRATE
IND  1  2 L^LBWO  !drain bondwires
MSTEP  2  22  W1=30  W2^WO  !step to line, W1 taken as width of set of drain bondwires
MLIN  22  3 W^WO  L^LO!matching line
MSTEP  3  4 W1^WO  W2^W51!step to 50 ohm line
MLIN  4  5 W^W51  L^LOR  !  length is (200 - LO) of 50 ohm line on matching substrate
MSTEP  5  6  W^W51  W2=22 !step between 50 ohm lines on substrates
MSUB ER=9.85 H=25 T=.2 RHO=1 RGH=0  !LAUNCH SUBSTRATE
MLIN  6  7 W=22  L=250!test fixture substrate
DEF2P  1  7  OUTPUT
!.................................................................................................................................
!OUTPUT LOAD BLOCK
CAP  1  0 C=1.6!output capacitance of 4.8mm HFET
OUTPUT  1  2
RES  2  0 R=50
DEF1P 1 HFLD  !defines load impedance presented to drain of HFET
!.................................................................................................................................
!COMPLETE AMPLIFIER BLOCK
INPUT 1  2
MODEL3  2  3
OUTPUT  3  4
DEF2P  1  4 AMP!complete amplifier
!.................................................................................................................................
FREQ
SWEEP  .01  8 1
SWEEP  7.5  9.5  0.1
SWEEP  9  17  1
!SWEEP  .5  10.5  .5
!.................................................................................................................................
OUT
  AMP  DB[S11]
  AMP  DB[S21]
```

```
  AMP  DB[S12]
  AMP  DB[S22]
  AMP  K
  AMP  DB[GMAX]
  HFLD  RE[Z11]
  HFLD  IM[Z11]
   !MODEL3  MAG[S11]
   !MODEL3  ANG[S11]
   !MODEL3  MAG[S21]
   !MODEL3  ANG[S21]
   !MODEL3  MAG[S12]
   !MODEL3  ANG[S12]
   !MODEL3  MAG[S22]
   !MODEL3  ANG[S22]
   !MODEL3  DB[GMAX]
   !MODEL3  K
!..............................................................................................................................
OPT
FREQ  8.5  8.5
!  HFLD RE[Z11]=9.5  !   TARGET LOAD RESISTANCE
!    HFLD  IM[Z11]=0
  AMP MAG[S11]=0
  AMP  DB[S21]>9.5
!END
```

DESIGN FILE OUTPUT

Frequency (GHz)	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	K AMP	DB[GMAX] AMP	RE[Z11] HFLD	IM[Z11] HFLD
0.010	-10.042	17.00	-66.663	-10.03	123.550	17.90	50.159	-0.49
1.010	-2.616	12.45	-33.092	-4.83	1.686	17.94	25.338	-24.50
2.010	-1.168	7.55	-32.101	-4.13	0.869	19.83	10.436	-18.87
3.010	-0.933	4.48	-31.800	-4.02	0.826	18.14	5.748	-13.17
4.010	-0.945	3.11	-30.869	-4.03	0.918	16.99	4.163	-9.28
5.010	-1.127	3.13	-29.138	-4.29	1.032	15.03	3.788	-6.48
6.010	-1.564	4.25	-26.667	-4.81	1.131	13.26	4.124	-4.27
7.010	-2.753	6.38	-23.420	-5.51	1.208	12.15	5.154	-1.38
7.500	-4.344	7.80	-21.507	-6.03	1.251	11.63	6.040	-1.52
7.600	-4.882	8.10	-21.104	-6.19	1.262	11.52	6.268	-1.35
7.700	-5.542	8.40	-20.704	-6.38	1.273	11.41	6.516	-1.19
7.800	-6.361	8.70	-20.314	-6.62	1.285	11.30	6.786	-1.03
7.900	-7.389	8.97	-19.942	-6.92	1.299	11.18	7.080	-0.88
8.000	-8.695	9.22	-19.597	-7.30	1.313	11.06	7.401	-0.74
8.100	-10.368	9.43	-19.292	-7.78	1.328	10.93	7.751	-0.61
8.200	-12.479	9.59	-19.040	-8.38	1.345	10.80	8.133	-0.50
8.300	-14.843	9.68	-18.853	-9.14	1.362	10.67	8.550	-0.40
8.400	-16.172	9.69	-18.744	-10.09	1.381	10.54	9.004	-0.34
8.500	-14.845	9.62	-18.722	-11.24	1.401	10.40	9.497	-0.30
8.600	-12.297	9.46	-18.791	-12.60	1.423	10.26	10.031	-0.31
8.700	-9.969	9.21	-18.949	-14.11	1.445	10.12	10.606	-0.37
8.800	-8.110	8.87	-19.190	-15.58	1.469	9.97	11.220	-0.49
8.900	-6.657	8.46	-19.503	-16.61	1.494	9.83	11.869	-693.00
9.000	-5.520	8.00	-19.876	-16.73	1.521	9.68	12.544	-0.99
9.100	-4.627	7.48	-20.294	-15.97	1.549	9.52	13.233	-1.39
9.200	-3.920	6.94	-20.745	-14.77	1.578	9.37	13.917	-1.91
9.300	-3.356	6.37	-21.219	-13.50	1.609	9.22	14.571	-2.57
9.400	-2.904	5.78	-21.705	-12.32	1.640	9.06	15.162	-3.36
9.500	-2.538	5.19	-22.198	-11.29	1.674	8.90	15.656	-4.29
10.000	-1.491	2.31	-24.592	-7.73	1.858	8.10	15.566	-9.98
11.000	-0.854	-2.66	-28.498	-4.45	2.332	6.45	7.505	-13.93
12.000	-0.688	-6.54	-31.213	-3.04	2.996	4.69	3.434	-11.61
13.000	-0.626	-9.71	-33.114	-2.38	3.950	2.80	2.016	-9.62
14.000	-0.617	-12.48	-34.529	-1.98	5.369	0.75	1.379	-8.27
15.000	0.690	-14.94	-35.574	-1.66	7.614	-1.49	0.997	-7.25
16.000	-0.765	-17.05	-36.251	-1.42	10.074	-3.43	0.767	-6.38
17.000	-0.698	-18.17	-35.936	-1.36	9.775	-4.02	0.679	-5.62

APPENDIX 2 HFET POWER AMPLIFIER DESIGN EXAMPLE

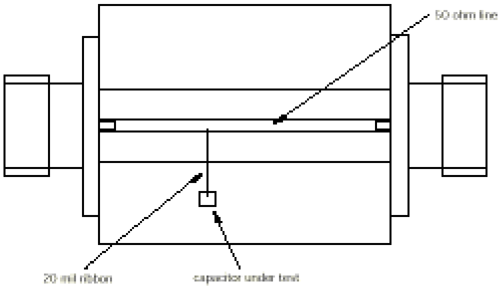
Series resistance of capacitors is a major contributor to the loss of matching networks, and it is strongly recommended to measure the ESR of any capacitors to be used in hybrid networks. Losses will vary from manufacturer to manufacturer, and from the same manufacturer when the parts (of the same value) are of different sizes.

It is relatively easy to measure the loss of a capacitor by incorporating it into a series resonant circuit in shunt with a transmission line, as shown below. Ideally the inductor should possess high Q, and should resonate the capacitor in the band of interest. Gold ribbon inductors are often a good choice.

The attenuation of the network is measured at resonance, and from this the ESR of the capacitor can be estimated from the data in the chart below. It will be a worst case value, since it will include a finite contribution from the inductor's series resistance.

If, after incorporating the measured ESR in the design file, the effect of the loss is too great, it will be necessary to rethink how the capacitor will be realized in the circuit. Often, a cure can be effected by using a number of smaller value capacitors in parallel. Alternatively, a different circuit may be required.

TEST FIXTURE FOR CAPACITOR LOSS MEASUREMENT



LOSS OF CAPACITANCE VS ESR In Series Resonant Circuit Zo = 50 Ohms