TriQuint SEMICONDUCTOR®

Advance Product Information
Application Note December 1, 2003

Maximum Input Power for GaAs MMICs

Background: TriQuint Semiconductor Texas has conducted tests to determine the maximum input power that can be applied to GaAs MMICs of three different processes. In many applications, devices may be subjected to higher input powers than the recommended normal operating conditions. It is understood that applications at greater than recommended input power may lead to degradation of device performance.

Method: Tests were performed on standard 300μm FET cells at different continuous wave input power levels ranging from 20dBm to 36dBm to determine a safe operating level of input power. All devices were tuned for maximum gain on the input and maximum power on the output.

An acceptable operating condition for input power is defined as a change of <10% in Gm, IDSS, Vp & breakdown voltage or a change of <1dB in gain.

Tests were performed for 16 hours each. Both DC and RF device characteristics were measured before and after the devices were subjected to high input power conditions. An input power that degraded any of the above parameters in excess of the stated allowable changes in performance was considered to be an unacceptable condition. Figure 1 below illustrates the test sequence.

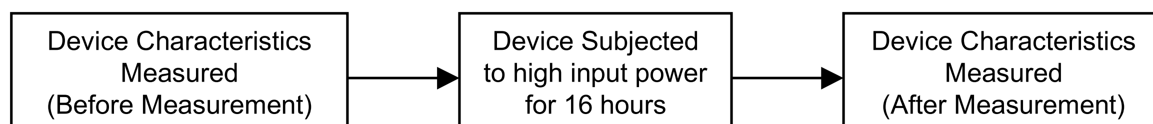

Figure 1 -- Device Test Flow Diagram

Results: Table 1 summarizes the DC and RF performance of 300μm standard FET cells after being subjected to the recommended high input power level for 16 hrs. All parameters remained within the acceptable degradation range. This data is used to calculate the maximum input power that TriQuint MMICs can safely withstand without unacceptable degradation. The maximum input power value that is listed on each TriQuint data sheet, reflects the acceptable input power level that may be applied without degradation in excess of that listed above.

It should be noted that device MTTF may be affected by long term exposure to high input power levels. Devices operated at or near maximum value for long periods of time may experience degraded performance or failure.

The results showed the following input power levels vs. input periphery:

- MESFET: 333mW/mm
- 0.25um pHEMT: 333mW/mm
- 0.15um pHEMT: 167mW/mm

Test Results of 300μm FET cells

DC & RF Parameter	0115101-5			0030704-2		
	Before	After	Change	Before	After	Change
Gm (mS)	60	60	0%	56	58	4%
Vp (V)	-1.26	-1.21	-4%	-1.09	-1.08	-1%
IDSS (mA)	56	54	-4%	44	45	2%
BVGD (V)	-20	-20	0%	-17	-18	6%
BVGS (V)	-16	-16	0%	-10	-11	10%
Gain @ Pin=+5.5dBm (dB)	11.29	11.4	0.11	9.06	8.94	-0.12

MESFET

Property	9928802-2			9933402-3			0006807-1		
	Before	After	Change	Before	After	Change	Before	After	Change
gm (mS)	80	80	0%	80	80	0%	80	80	0%
Vp (V)	-0.98	-0.92	3%	-0.96	-0.98	-1%	-0.94	-0.95	-1%
Idss (mA)	61	65.75	-4%	67.2	68.19	-1%	59.63	65.21	-4%
Vbrgd (V)	-15	-15	0%	-18	-18	0%	-19	-18	3%
Vbrgs (V)	-14.5	-14	2%	-18.5	-18	1%	-18	-17	3%
Vgsq (V)	-0.33	-0.37	-6%	-0.477	-0.488	-1%	-0.352	-0.400	-6%
Gain @ Pin=9.5dBm (dB)	10.85	10.85	0.00	10.98	11.01	-0.03	11.26	11.28	-0.02
Gain @ Test Power (dB)	2.48	2.47	0.01	1.79	1.78	0.01	2.15	2.2	-0.05

0.25um pHEMT

Property	9928802-2			9933402-3			0006807-1		
	Before	After	Change	Before	After	Change	Before	After	Change
gm (mS)	28	30	-7%	30	28	7%	26	28	-8%
Vp (V)	-0.36	-0.33	8%	-0.39	-0.38	3%	-0.35	-0.33	6%
Idss (mA)	9	9	0%	11	10	9%	8	8.5	-6%
Vbrgd (V)	-11	-11	0%	-7	-7	0%	-8.5	-8.5	0%
Vbrgs (V)	-11	-11	0%	-7	-7	0%	-8.5	-8.5	0%
Gain @ Pin=9.5dBm (dB)	8.26	8.1	0.16	9.7	9.16	0.54	8.76	8.22	0.54
Gain @ Test Power (dB)	1.54	1.46	0.08	3.86	3.48	0.38	3.15	2.62	0.53

0.15um pHEMT