ESD Sensitivity of TriQuint Texas Processes and Circuit Components

GaAs semiconductor devices have a high sensitivity to Electrostatic Discharge (ESD) and care must be taken to prevent damage. This document provides typical Human Body Model (HBM) failure thresholds for individual circuit components. Based on the data below and careful examination of a circuit, its overall ESD sensitivity can be assessed by finding the least robust component of the circuit.

The most ESD sensitive components in a typical GaAs MMIC are:
a) small Field Effect Transistor (FET) devices,
b) small Schottky diodes,
c) small MIM (Metal-Insulator-Metal) capacitors,
d) narrow gaps of isolated substrate between metal lines at a different potential.

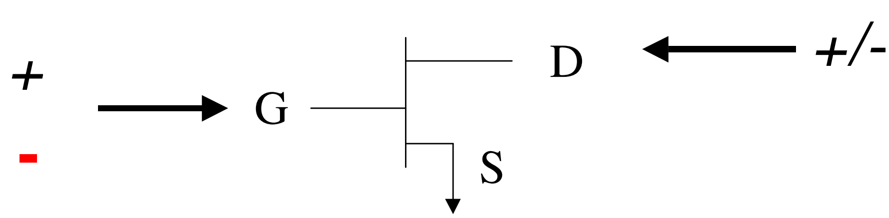
1 Field Effect Transistors

In the typical common source configuration, FET devices are most vulnerable to negative discharges to the gate. FET devices can handle somewhat greater positive discharges to the gate, and positive or negative discharges to the drain. In all cases, ESD sensitivity is strongly dependent on gate width.

1.1 General Characteristics

ESD sensitivities are described in the figure below for the typical common-source FET configuration.

- Positive discharges to the gate can be conducted through the Schottky gate junction if the gate width is sufficiently large.
- Positive or negative discharges to the drain can be conducted through the FET channel if the gate width is sufficiently large.



- *Greatest vulnerability is for negative discharges into the gate.*
- For any terminal and polarity, ESD sensitivity scales with gate width. Smaller devices are more vulnerable.

1.2 Typical Failure Thresholds: Discharge to the Gate

The ESD test procedure is to perform HBM discharges at a given voltage and then check for damage. The test voltage is raised in 50V increments. Typical failure thresholds for positive and negative discharges to the gate are listed below for 300 µm FETs.

Process type	Failure threshold, Positive G-S discharge, V	Failure threshold, Positive G-D discharge, V	Failure threshold, Negative G-S discharge, V	Failure threshold, Negative G-D discharge, V
0.5 µm HFET 2MI	1200	1150	-230	-300
0.35 µm PWR pHEMT 3MI	1020	970	-200	-200
0.25 µm mmW pHEMT 3MI	950	1030	-150	-170
0.15 µm PWR pHEMT 3MI	780	750	-130	-150
0.15 µm LN mHEMT 3MI	700	1100	*	*

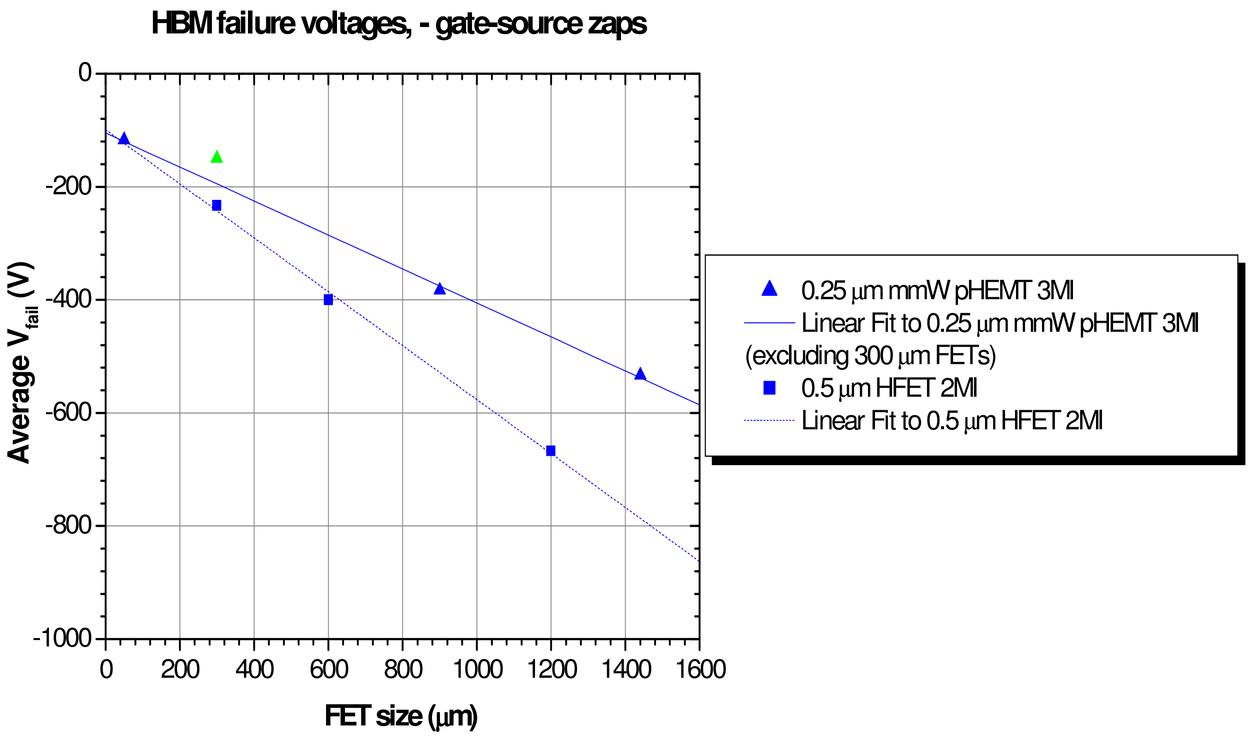
* Failed after first 50 V step

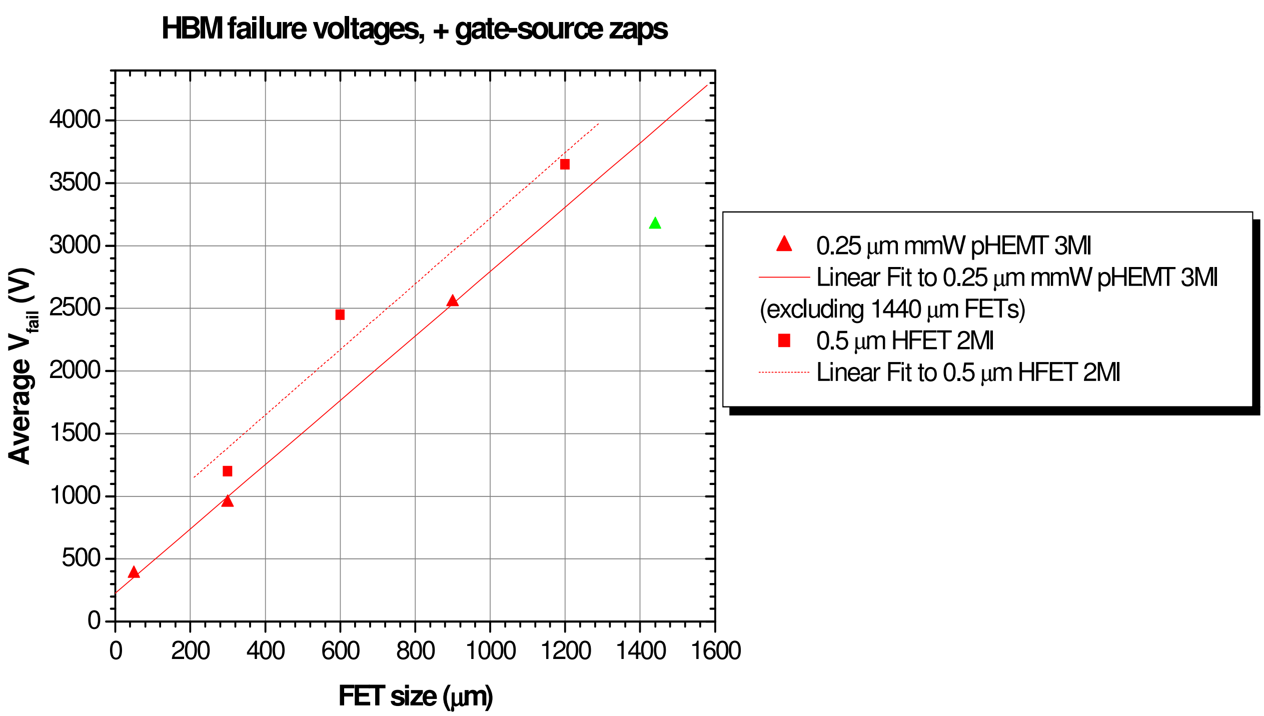
All processes are much more sensitive to negative discharges on the gate. The mHEMT process is particularly sensitive to negative discharges; mHEMT devices failed after the initial -50 V step. On the other hand, mHEMT devices can handle positive discharges to the gate at levels similar to other technologies.

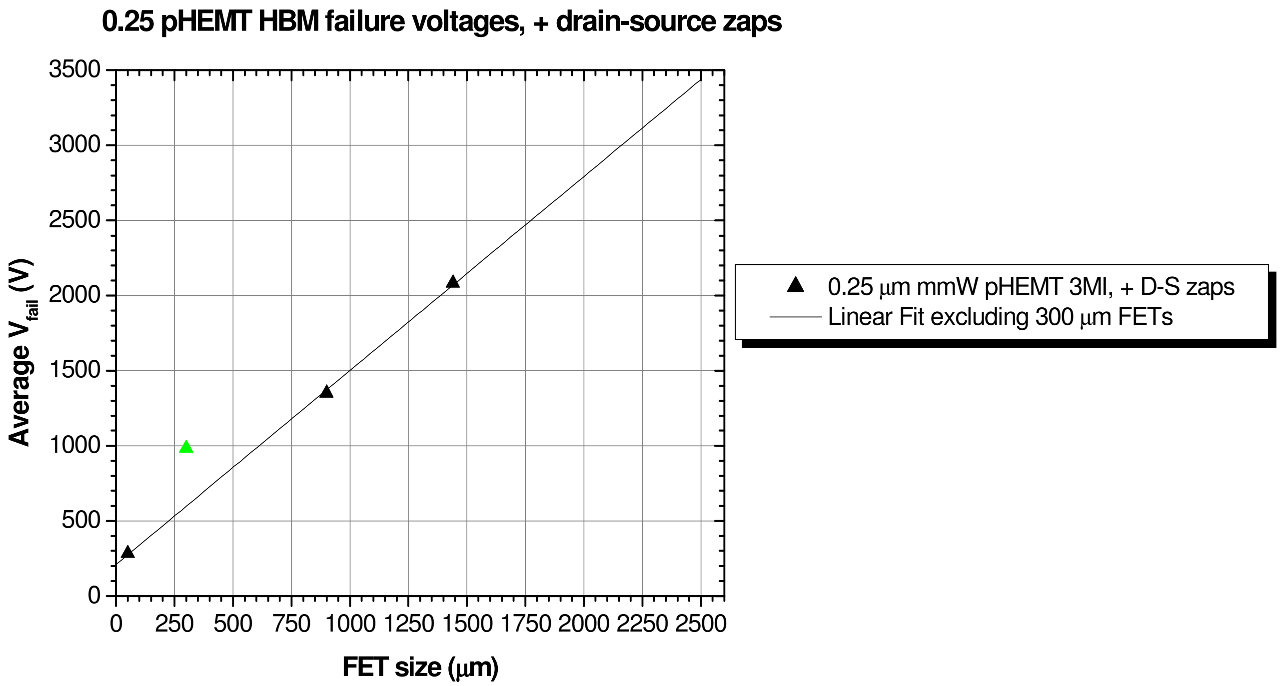
Also note that wrist straps, commonly used to minimize ESD when handling sensitive devices, are typically specified to limit ESD levels to 200 V or less. Clearly, 200 V is not adequate for 300 µm pHEMT and mHEMT devices.

1.3 Scaling of ESD Sensitivity with FET Gate Width

ESD sensitivity decreases as gate width is increased. HBM failure voltages are directly proportional to FET size. Very small devices, < 200 µm, are extremely sensitive. Data shown below is for positive and negative discharges, Gate-Source and Drain-Source. The HBM discharge is applied across two terminals, with the other terminal floating. Gate leakage is monitored to determine failure. Negative discharges to the gate typically result in an abrupt catastrophic failure. On the other hand, positive and negative Drain-Source and positive Gate-Source and Gate-Drain discharges can cause gradual increases in gate leakage without causing catastrophic failure. The data below are for voltage levels that resulted in less than 1 kΩ of gate resistance.

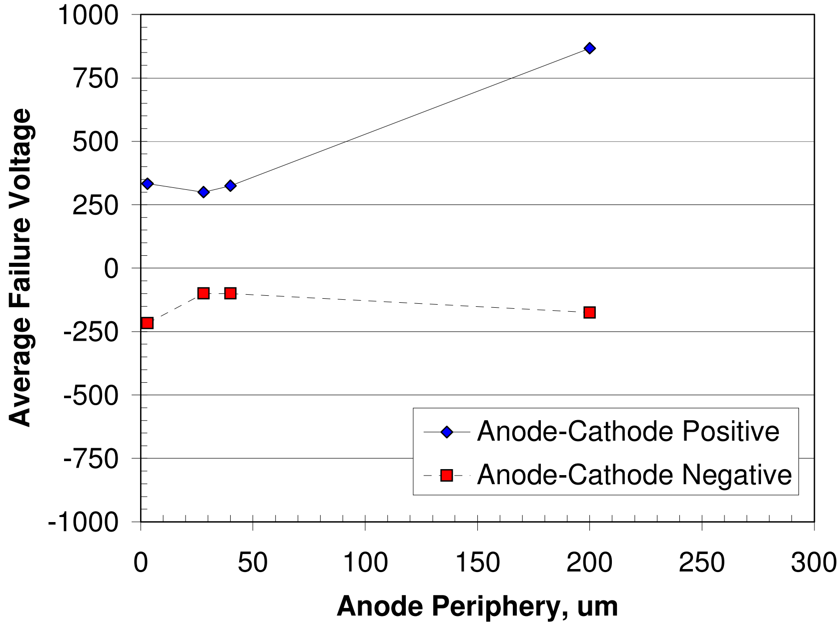

HBM failure voltages, - gate-source zaps
Average V_{fail} (V)
FET size (µm)
0
-200
-400
-600
-800
-1000
0
200
400
600
800
1000
1200
1400
1600
0.25 µm mmW pHEMT 3MI
Linear Fit to 0.25 µm mmW pHEMT 3MI
(excluding 300 µm FETs)
0.5 µm HFET 2MI
Linear Fit to 0.5 µm HFET 2MI


HBM failure voltages, + gate-source zaps
Average V_{fail} (V)
FET size (µm)
4000
3500
3000
2500
2000
1500
1000
500
0
0
200
400
600
800
1000
1200
1400
1600
0.25 µm mmW pHEMT 3MI
Linear Fit to 0.25 µm mmW pHEMT 3MI
(excluding 1440 µm FETs)
0.5 µm HFET 2MI
Linear Fit to 0.5 µm HFET 2MI



2 Diodes

ESD sensitivity of diodes is similar to that of FETs. Typical data for 4 µm diodes fabricated in the 0.25 µm pHEMT process are shown below. Very small diodes are vulnerable to positive and negative discharges to the anode. Larger periphery diodes can be used as protection devices for positive discharges to the anode.

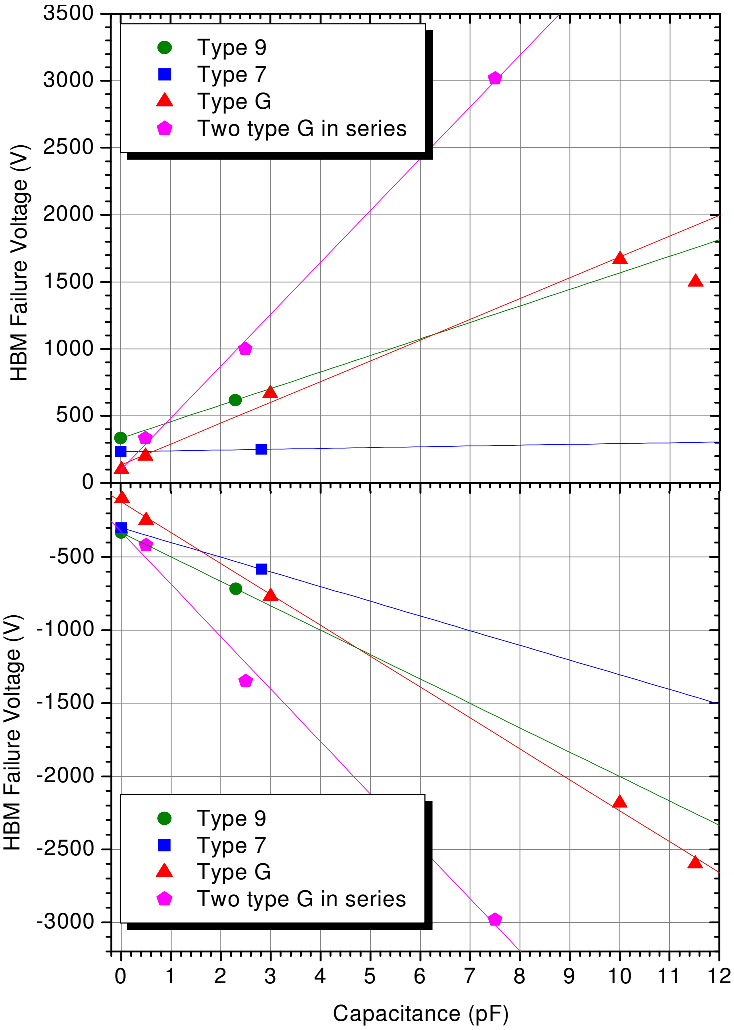


3 TaN Resistors

Based on TLP (Transmission Line Pulse) data, TaN resistors can handle for short time intervals (100 ns) typical of HBM ESD transients significantly higher current densities than the DC current limits. TaN resistors remain fairly constant in value during high current transients with a very slight resistance drop just prior to failure. The transient failure current density of TaN resistors depends on the physical size of the resistor, with large resistors failing at lower current densities than small resistors.

4 Capacitors

ESD sensitivity of capacitors depends on dielectric thickness and is a linear function of capacitor size for a given capacitor type. The 3MI process includes three capacitor types: Type G (1200 pF/mm^2), Type 7 (300 pF/mm^2), and Type 9 (240 pF/mm^2). The 2MI process includes one type of capacitor similar to the type 7 3MI capacitor. Note that for small sizes, Type G is the most sensitive, while for large sizes, it is the most robust type of capacitor. During the ESD event, a large area Type G capacitor has enough conductivity in the dielectric to dissipate the ESD charge, providing a measure of self-protection. The figure below illustrates the behavior of type G, 7, and 9 capacitors as a function of increasing capacitance (area), as well as the fact that using 2 capacitors in series results in doubling the HBM failure voltage compared to a single capacitor with the same total capacitance.



5 Isolated Substrate Gaps

Isolated substrate gaps between metal lines at a different potential are as sensitive to ESD as any other circuit component. Spacing between metallization on the circuit needs to be optimized for achieving the desired ESD robustness level. Our test results suggest that a safe scaling rule is 30 V HBM voltage per micron of spacing.

6 References

1. J. M. Beall and G. I. Drandova, *ESD Protection for pHEMT MMIC Amplifiers*, 2005 Compound Semiconductor Integrated Circuit Symposium Technical Digest, p. 276, 2005.

2. G. I. Drandova, J. M. Beall, and K. D. Decker, *SiN Capacitors and ESD*, 2006 MANTECH Technical Digest, p. 83, 2006.