RF Module Assembly Overview

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Abstract

Over the years, the electronics industry has constantly been driven to produce components that incorporate multi-functionality and miniaturization, while maintaining improved reliability and low cost. While the portfolio of single die packages can still produce revenue for compound semiconductor companies today, the RF packaging momentum has taken a huge swing towards organic, multi-layered, substrate modules with multiple component integration and miniaturized footprints. Successful volume assembly of these high performance components (often referred to as "System In Package" or SiP modules), is key and requires good substrate design rules, proper material selection, specialized manufacturing equipment and assembly processes, improved process controls, and flexible assembly and test partners.

INTRODUCTION

By definition, a module is "a self-contained component of a system, which has a well defined interface to the other components" [1]. *RF Module Packaging* or *System in Package (SiP)* are terms used to describe the functional integration of semiconductor devices (elemental and/or compound), Surface Mount Devices (SMDs), Integrated Passive Devices (IPDs), substrate, SAW filters, and even EMI shields. This paper focuses on interconnect methodologies specific to wire bond and flip chip RF modules, using organic laminates and overmold encapsulation. It is also intended to providing a basic understanding of module assembly to all those who have an interest in producing reliable, high performance, low cost RF modules.

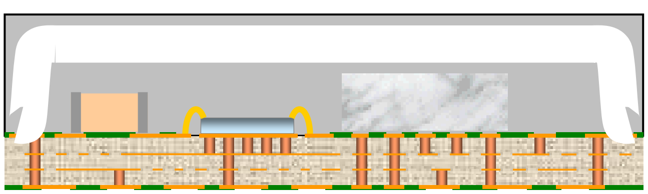

FIGURE 1. SIP MODULE SHOWING INTEGRATION OF COMPONENTS [2]

RF SUBSTRATE CONSIDERATIONS

As the evolution of RF modules continues to migrate towards smaller and smaller outlines, the role of the substrate as a component in the overall system becomes more and more significant. The substrate must be regarded as another critical component, not just a carrier that supports die and other devices. Special attention must be given to material properties, laminate construction, and processing tolerances when tuning for optimum performance. Material set selection should also include consideration of other factors such as Cu thickness at each metal layer, trace width tolerance (top and bottom of trace), via structures, prepreg thickness, surface finish and plating thickness, solder mask placement, proximity of features relative to other features, and placement of ground planes.

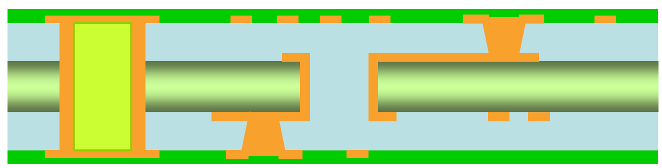

FIGURE 2. SECTION VIEW OF A 4-LAYER SUBSTRATE

DESIGN RULES

Substrate Design Rules play a significant role in the success of RF module designs. The main objective is simply to provide design and assembly teams with current information that aligns performance optimization needs with current manufacturing processes and capabilities. That said, if a designer's rule sets are wrong, unclear, or outdated, it could directly impact directives to produce a product that meets company objectives for reliability, high performance, and/or low cost.

Another added benefit to having good design rules is that it also serves as the basis against which design reviews are measured. If rules are unclear, it could make design reviews much more complex than they need to be, especially if the rules are built in to an automated DRC (Design Rule Check) system.

As with any product, the challenge is then to provide effective RF substrate rules that produce competitive, reliable, manufacturable, low cost designs. Although necessary, this task is constant, arduous, and never ending. Due diligence to constantly track multiple substrate supplier and assembly capabilities will help to ensure that designers are provided the latest, and most advanced options. Note that caution must also be exercised, as the temptation to implement rules that appear to offer an immediate advantage, but have not yet been proven to be valid, exists frequently. In such cases, the segregation of rules into categories of risk and/or *Best Practices* should be utilized.

Wire Bonding vs. Flip Chip for RF Designs

Many factors are considered when deciding upon which interconnect method is best. While wire bonding is still the most dominant method due to lower cost and design flexibility, flip chip is quickly becoming more popular, mainly due to opportunities in reduced package outlines, advances in process stability, and progressive reduction in flip chip assembly costs.

Wire Bonding Technology - Briefly Described

Ball bonding, the most common form of wire bonding, is a process by which Au wire (sometimes as thin as 15um in diameter) is used to weld a connection between die pads and substrate bond fingers. The process first involves the formation of a Au ball created by EFO (Electronic Flame Off), after which it is then lowered to the bonding surface and then attached using a combination of ultrasonic energy, heat, and pressure. The capillary (or needle) through which the wire is fed, utilizes a sequence of clamping actions to then direct the wire to the lead to create the tail bond. The cycle is then repeated for subsequent multiple bonds.

The following diagram describes the capillary ball bonding cycle, showing how the ball and tail bonds are created.

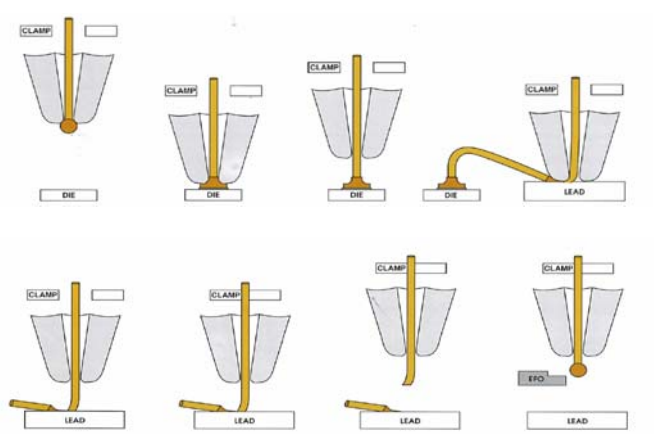

Figure 3. CAPILLARY Wire Bonding Cycle [4]

SiP Process Flow – WireBonding

The process flow for any SiP module will encompass strategies that take assembly materials, equipment, manufacturing processes, inspection, material transport, and other processing requirements into careful consideration. A typical SiP Wire-Bond process flow consists of three main sections: SMD Attach, FOL (Front of Line) assembly, and EOL (End of Line) assembly.[2]

SMD Attach

1. Screen Printing
   Placement of solder paste onto SMD pads
2. Component Mount
   Chip Mounting of SMDs onto printed paste
3. Reflow
   Reflow soldering to attach SMDs to substrate
4. Aqueous Clean
   Remove flux residue and contaminants
5. SMD Final Visual Inspection
   Inspect for anomalies

FOL (Front of Line)

6. Wafer Mount/Saw
   Mount wafer onto taped ring/singulate
7. 2nd Optical
   Perform die visual inspection for defects
8. Multiple Die Attach
   Dispense epoxy, place multiple die
9. Die Attach Cure
   Bake to cure the epoxy
10. Plasma Clean
    Prep clean the wire bond pads for bonding
11. Wirebond
    Au ball bonding to connect die pads to components
12. 3rd Optical
    Inspect for anomalies

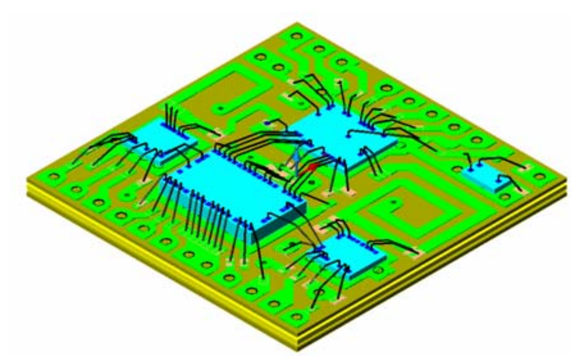

Figure 4. SiP module after wire bonding

EOL (END OF LINE)

13. Shield Attach (Optional)
    Place epoxy, attach shield
14. Shield Cure
    Bake to cure the epoxy
15. Plasma Clean
    Prep clean for mold encapsulation
16. Mold (vacuum)
    Encapsulate strip with mold compound, snap cure
17. Post Mold Cure
    Final Cure of mold compound
18. Laser Mark
    Laser etch mark the mold compound
19. Ball Attach (Optional)
    Attach solder balls to module
20. Singulate
    Saw to singulate each unit from strip form
21. Final Visual Inspection
    Inspect for anomalies

FIGURE 5. FULLY ASSEMBLED SIP MODULES

FLIP CHIP TECHNOLOGY – BRIEFLY DESCRIBED

Flip chip interconnect can be described as an “advanced form of surface mount technology, in which bare semiconductor chips are turned upside down, and hence called *flip chip*, (i.e. face down), and bonded directly to a printed circuit board or chip carrier substrate.”[5]

The volume of flip chip assembly in RF modules is rapidly increasing, especially since advancements in process development and stabilization have helped to address the pricing parity that existed between flip chip and wire bond assembly. Although the advantages of flip chip technology over wire bonding are evident (electrical and thermal performance, form factor reduction, process stability, etc), the complexity that comes with tuning RF circuits is still a challenge that results in multiple design iterations. To explain further, when considering wire bonding, performance tuning during prototype development could be achieved with simple changing of wire lengths or moving of die, but flip chip interconnects are fixed and limit tuning opportunities to changes within the substrate design.

Nevertheless, if designers are successful in working through these tuning challenges, and if assembly suppliers can couple that with advances in process development, the resulting module can bring advantages that are hard to compete with.

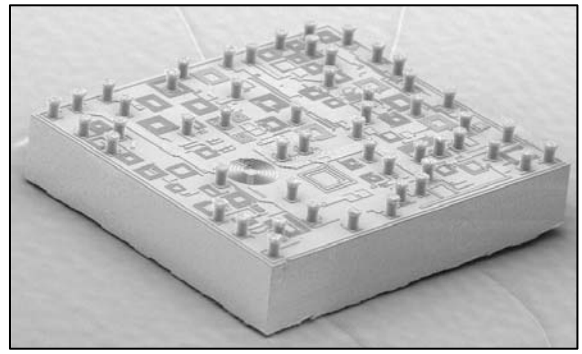

FIGURE 6. FLIP CHIP GAAS DIE WITH CU PILLAR INTERCONNECTS

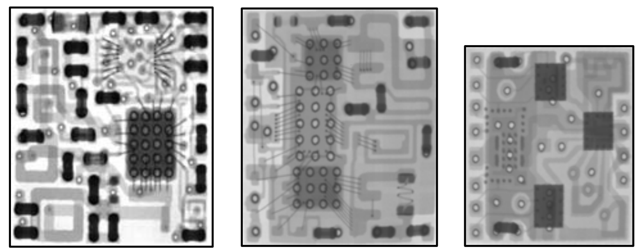

FIGURE 7. TRIQUINT’S FLIP CHIP PART (FAR RIGHT) ESTABLISHES THE ADVANTAGE OVER ITS COMPETITOR’S WIRE BONDED VERSIONS.

A typical SiP Flip Chip Process flow also has 3 sections: [2]

SMD ATTACH

1. Screen Printing
   Placement of solder paste onto SMD pads
2. Component Mount
   Chip Mounting of SMDs onto printed paste
3. Reflow
   Reflow soldering to attach SMDs to substrate
4. Aqueous Clean
   Remove flux residue and contaminants
5. SMD Final Visual Inspection
   Inspect for anomalies

FOL (FRONT OF LINE)

6. Wafer Mount/Saw
   Mount wafer onto taped ring/singulate
7. 2nd Optical
   Perform die visual inspection for defects
8. Flip Chip Attach
   Flux, align, reflow
9. 3rd Optical
   Inspect for anomalies

EOL (END OF LINE)

10. Shield Attach (Optional)
    Place epoxy, attach shield
11. Shield Cure
    Bake to cure the epoxy

12. Plasma Clean
    Prep clean the strip for mold encapsulation
13. Mold (vacuum)
    Encapsulate the strip with epoxy, snap cure
14. Post Mold Cure
    Final Cure of mold compound
15. Laser Mark
    Laser etch mark the mold compound
16. Ball Attach (Optional)
    Attach solder balls to module
17. Singulate
    Saw to singulate each unit from strip
18. Final Visual Inspection
    Inspect for anomalies

Other Considerations

Outside of deciding which interconnect method best suits the intended module, the following should also be taken into consideration:

- Materials
  Component materials, assembly materials, processing materials will all have an affect on the success or failure of a part.
- Vendor
  In addition to capability assessment, when selecting a vendor, look for one that is flexible, especially during the development phase. A good vendor will make periodic visits to ensure product development and/or production issues are being addressed in a timely manner. Presentations on roadmaps and advanced capabilities are also signs that a vendor is interested in building a long lasting and successful relationship.

Conclusion

Successful methodologies for assembly of small scale RF modules exist, requiring careful consideration of materials, processes, and techniques. Strong supplier relationships will also be key to keeping up with the latest capabilities, developing roadmaps, and in working closely together to produce quality product. Lastly, an understanding of the basic assembly process is key to anyone who has any part or responsibility for delivering products that are reliable, manufacturable, and low cost.

Acknowledgements

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References

[1] *Definition of a Module*, Wikipedia, February 2008.

[2] David Bolognia, *System in Package Presentation*, Amkor Technology November, 2007.

[3] Gregory Phipps, *Wire Bond vs Flip Chip Packaging*, Advanced Packaging Magazine, July 2005.

[4] *PECO Semiconductor Production Parts Catalog*, PECO, Seoul, Korea, 1997

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