FEATURE

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PHEMTs rise to wide-gap challenge

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New geometries and field plates have extended the operating voltage, power output and efficiency of GaAs PHEMTs to a level where they can compete with SiC and GaN-on-silicon devices, claim David Fanning, Edward Beam, Paul Saunier and Hua-Quen Tserng from TriQuint Semiconductor.

Process enhancements can extend the lifetime of cost-effective incumbent technologies and enable them to fight off the threat from new alternatives. Silicon LDMOS amplifiers, for example, have improved in performance, thanks to process advances to fend off rivalling compound semiconductor products. Similarly, GaAs amplifiers are now raising their voltage and power as wider-bandgap technologies come on the scene.

TriQuint Fab

Since GaAs was developed, its operating voltage has generally been restricted to less than 10V. However, military and commercial base-station applications have driven demand for higher power-output densities, which has led to higher-voltage GaAs processes. At the same time, GaN technology has raised the bar in terms of operating voltage and power-output density. This material has inherent advantages over GaAs, but our results have revealed that it is possible to extend the operating voltages and power-output densities of GaAs further.

Even with these improvements, GaN-on-SiC holds advantages over GaAs in some areas, such as power density and higher-frequency operation. However, GaAs can offer process maturity and proven reliability at a reasonable cost. These benefits are very important in risk-averse markets, such as defense, where RF transistors are used for radar and communications, as well as the cellular-base-station sector. So for systems requiring near-term deployment, decision makers must weigh the maturity, performance and cost of GaAs versus GaN.

Our recent improvements to GaAs performance began with our 0.35μm power PHEMT process (PWRPHEMT), which we reported in 2002 and released two years later. This extended the operating voltage of GaAs PHEMT amplifiers to 12V for frequencies of up to 18GHz. More recently, a modified version of this process, HV3X, has been optimized for power output in the X-band (8–12GHz). This design delivers 2.0W/mm – twice the power-output density of conventional GaAs – at a power-added efficiency (PAE) of 55% at 10GHz.

We have also developed an HV3S production process that delivers an operating voltage of up to 28V, alongside high PAE and high power-output density at S-band frequencies (2–4GHz). High voltages can be combined with low current operation to produce system efficiency improvements. A high PAE is required at these powers to combat the relatively poor thermal conductivity of the underlying GaAs substrate. By maintaining a suitable PAE, channel temperature and power dissipation are kept to acceptable levels. This process and the HV3X and PWRPHEMT processes are being used for both internal and foundry designs that can serve military applications and cellular infrastructure. Meanwhile, process development currently under-way has demonstrated operation up to 48V.

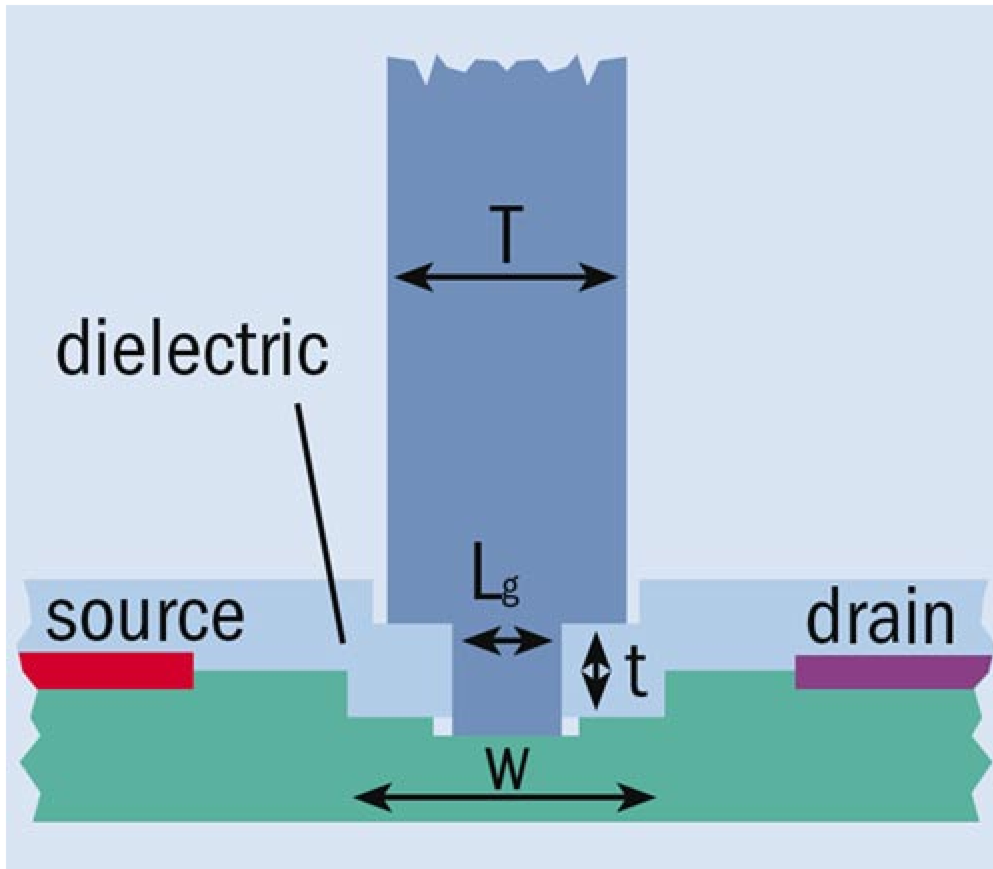

Figure 1

Adding field plates

The first target for our HV3S process was an increase in the operating voltage from 15 to 28V. Unfortunately the higher operating voltage comes at the expense of current handling and cut-off frequency. Taking HV3X as the starting point, we modified a T-shaped field plate (figure 1), and increased and optimized the channel geometry. The overlapping gate serves as an integrated field plate and holds the key to reducing the peak electric field in the channel. By cutting the electric-field strength here, the operating voltage is greatly increased at the expected penalty of diminished frequency response.

Our HV3S process uses identical techniques for metallization and capacitor fabrication to those employed for our established three-metal interconnect (3MI) technology. The epitaxial structure is also similar to our conventional PHEMTs, but it is modified to reduce leakage current at high voltages. At 15V or more, conventional devices suffer from leakage through the substrate, which

degrades the PAE, but the new structure maintains a high PAE up to 40 V. As expected, our HV3S process leads to lower current and transconductance due to a larger gate length and wide recess. Typical values for maximum transconductance and maximum drain current are 250 mS/mm and 450 mA/mm, respectively, compared with values of 400 mS/mm and 600 mA/mm for our 12 V process.

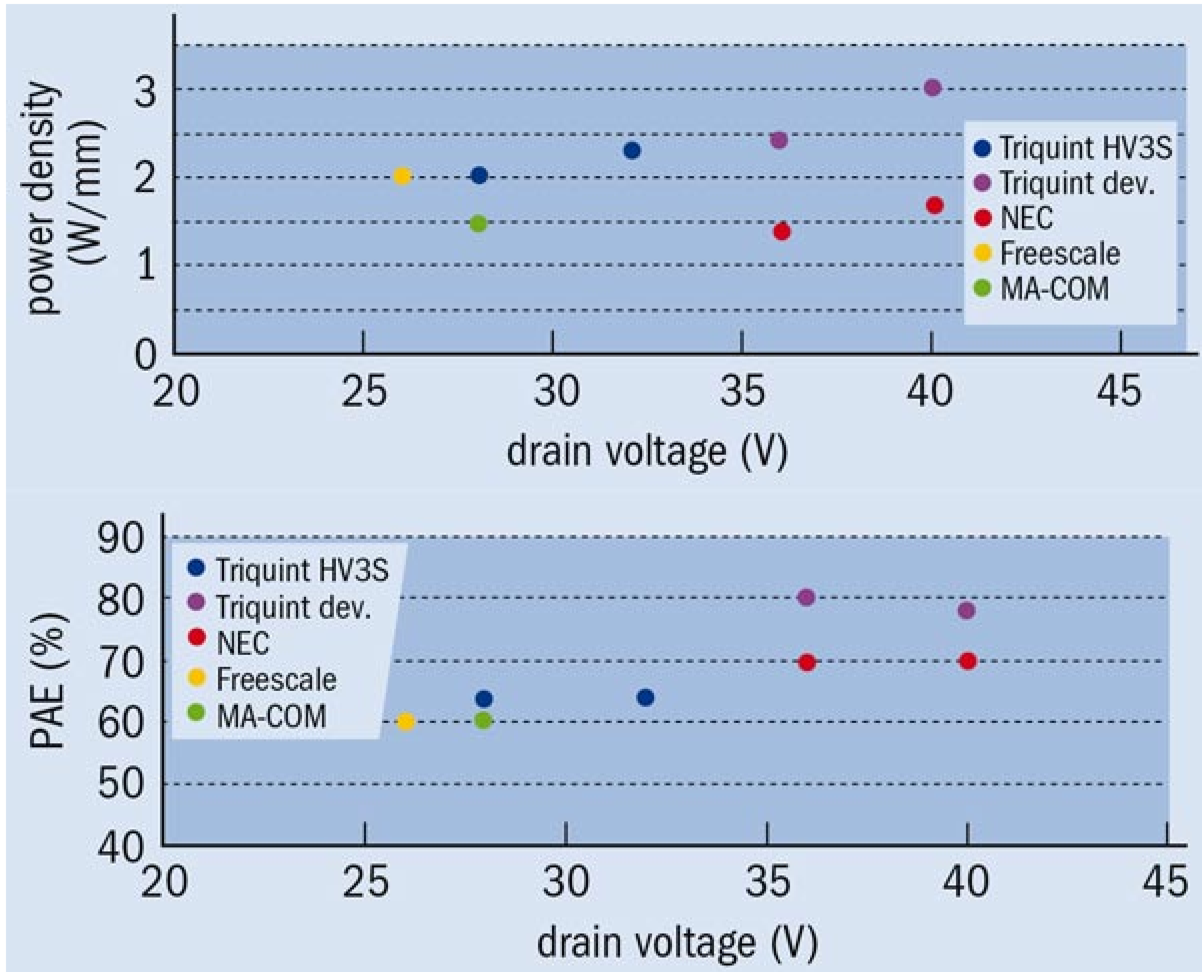

Figure 2

RF load-pull performance measurements at 3.5 GHz on a 4 × 250 μm device reveal a power density of 2.1 W/mm, 14 dB gain, a cut-off frequency of 7 GHz and 64% PAE at 28 V. These figures, which are tuned for maximum efficiency and quote power at the peak PAE, compare favorably with other GaAs PHEMT manufacturers that have developed high-voltage PHEMTs (figure 2).

Several MMICs have been designed using the HV3S process. Most are customer owned or competition sensitive, but there is an exception: a single-stage "reliability MMIC" with 4.8mm of gate periphery, which is suitable for performance monitoring and reliability testing. This MMIC was not designed for high PAE, but it does demonstrate the power capability of this type of chip. At 24V it delivers 7–8W between 2.6 and 3.4GHz at a PAE of 45–51%. The power-output density varies from 1.7W/mm at 24V to more than 2W/mm at 32V, which is similar to the 1mm discrete load-pull results. The power and PAE values are also nearly identical to those reported in 2004 for a 4.8mm SiC MESFET built by George Henry and co-workers from Northrop Grumman, while the gain is about 2dB higher.

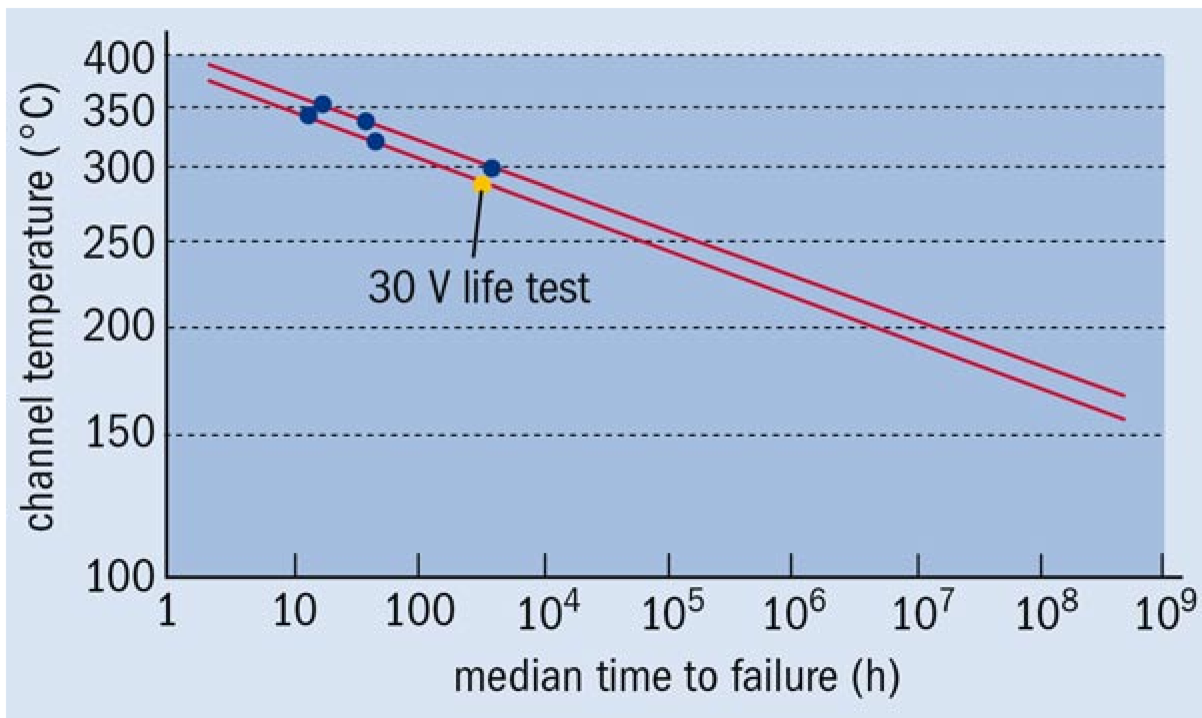

Figure 3

It's imperative to verify that the hike in operating voltage produced by the HV3S process does not come at the expense of any new failure mechanisms. Encouragingly, reliability tests that accelerate temperature and operating voltage reveal that HV3S' temperature performance is superior to that of our conventional GaAs, thanks to the enlarged channel parameters and lower current sensitivity. Predicted lifetimes of a million hours at a channel

temperature of more than 200 °C were drawn from an Arrhenius plot that shows a thermal activation energy of 1.9 eV (figure 3). Even at an operating voltage of 30 V, no voltage-accelerated degradation is seen in the data. The lower temperature tests lasted more than 3000 h to expose any lower-activation-energy failures. Using a single-stage reliability MMIC, RF life tests were performed at 24, 27 and 30 V at a reduced channel temperature to focus only on electrical effects. None of the devices degraded during the 2000 RF life hour test and no differences due to operating voltage were observed.

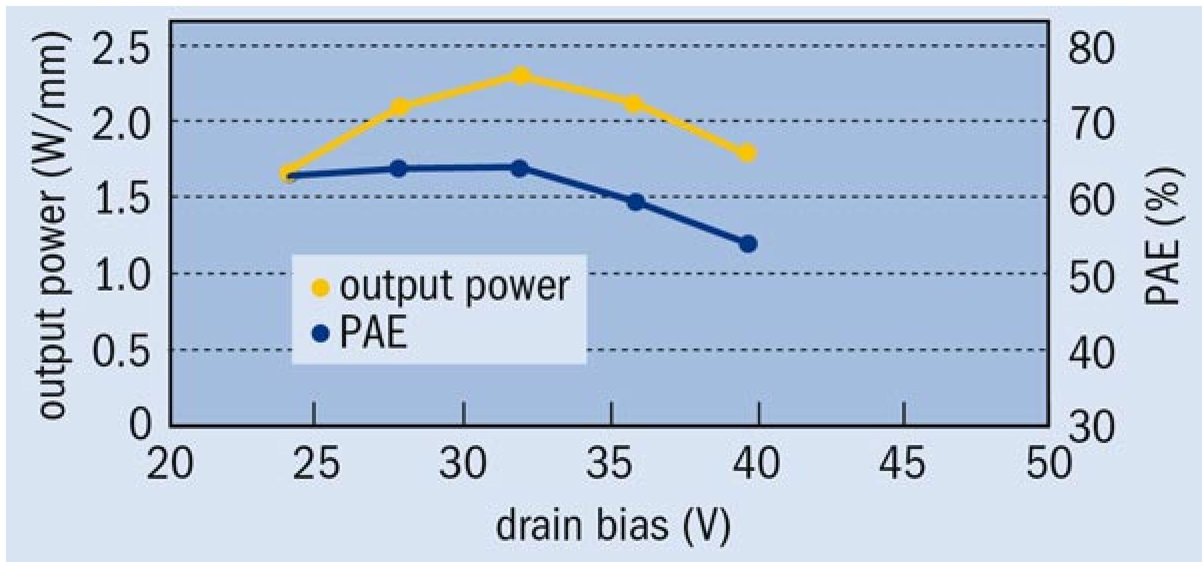

Figure 4

Our high-voltage PHEMTs also deliver robustness, according to qualification tests that involve the load pulling of every wafer at 28 V to verify voltage-handling capability and performance. Measurements showed very consistent results, with standard deviations of 5% and 2% for the power and PAE measurements, respectively. Load-pull tests were also taken at higher voltages until the device failed. These revealed that a 4 × 250 μm device typically delivers 2.3 W/mm and 65% PAE at 32 V, and survives all the way to 40 V. Similarly, we have conducted on-wafer and in-fixture tests of MMICs at over-voltage conditions, which survived to 36 V – the upper limit of our testing apparatus.

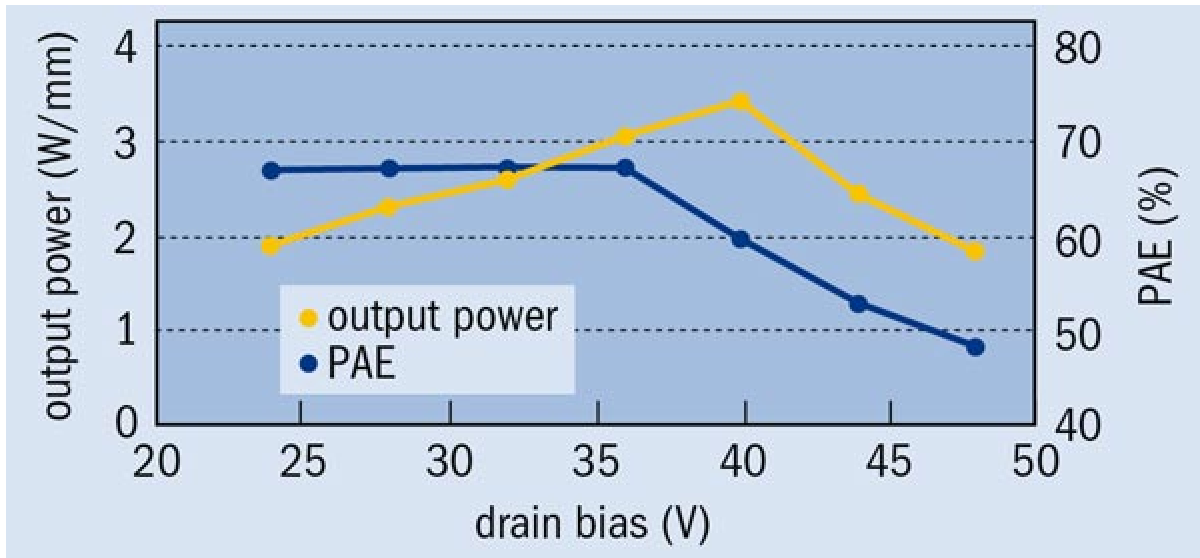

Figure 5

We are currently developing a new process for even higher voltage, power-output density and PAE. Further modifications to the channel and epitaxial structure have led to 48V operation and an increase in the PAE by typically 5%. With these adjustments, power-output densities of 3.4W/mm at a PAE of 60% have been delivered at 40V bias on a 4×250μm device (figure 5).

These gains in output-power densities have demanded comparable improvements in PAE to maintain reliable channel temperatures and can be met by tuning the second and third harmonics. Effects of harmonic impedance on efficiency are well known and amplifiers configured in the class B, over-driven class B, class C, class E and class F mode can all deliver efficiency enhancements. In each case, reactive terminations functioning at harmonic frequencies shape the current and voltage waveforms at the device terminals. For greatest success, overlap between the current and voltage must be minimized to avoid power dissipation that hampers DC to RF conversion efficiency. The load must also be optimally matched at the fundamental frequency for high-efficiency operation. Efficiency improvements with this technique are significant – predictions show drain efficiencies in excess of 80% using optimum terminations for only the second and third harmonics.

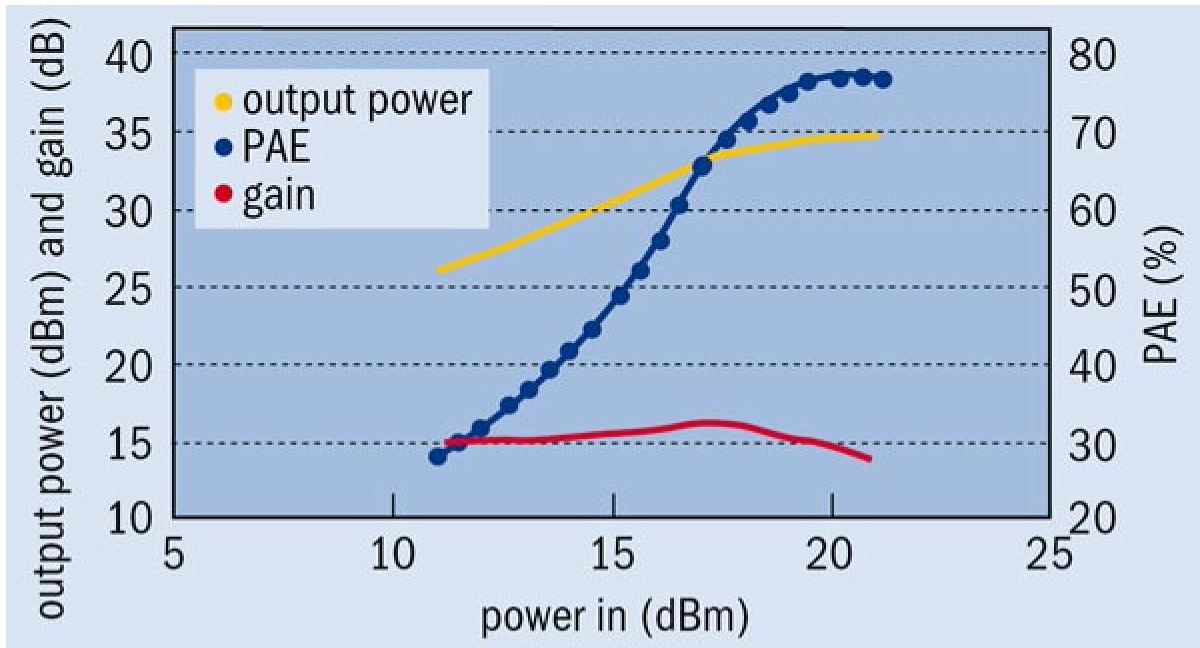

Figure 6

Accounting for harmonics

By short-circuiting the second harmonic and using an open circuit at the third harmonic for both the input and output, we have produced a 4 × 250 µm device biased at 40 V that delivers 78% PAE, 14 dB gain and 3.0 W/mm output at 3.5 GHz (figure 6). At a reduced drain voltage of 36 V, the PAE of this class F device increases to 80% with 13 dB gain at 2.42 W/mm. The drain efficiency is 84%, which is very close to the theoretical efficiency of a type of transistor operating in this mode. Harmonic terminations can also be performed on an MMIC, typically at the expense of bandwidth. In the production HV3S process, harmonic tuning enabled 2.1 W/mm and 72% PAE at 32 V.

The performances delivered with our latest process, such as 3.4 W/mm and 60% PAE at 3.5 GHz using 40 V operation, are comparable to SiC and GaN-on-silicon devices. For example, Cree's 1 mm SiC devices operating at 50 V produce 3.4 W/mm and 60% PAE at 3.5 GHz, while Nitronex's GaN-on-silicon FETs deliver 3.9 W/mm and a 62.5% drain efficiency, at 28 V and 3.5 GHz. GaN-on-SiC technology can deliver even better power performance. Published results of S-band frequencies include 5.4 W/mm at 28 V and 10 W/mm at 48 V, and the

technology has the potential to go to even higher voltages. More important, GaN-on-SiC delivers high power and PAE at much higher frequencies than any high-voltage GaAs technology. However, for SiC and GaN-on-silicon, frequency performance is more limited. For SiC, the low cut-off frequency limits its upper range to the S-band, while GaN-on-silicon technology has focused on lower frequencies for commercial markets. We have demonstrated X-band operation in GaN-on-silicon devices, but found that RF losses in the substrate will restrict performance at higher frequencies. Since both of these types of device offer a comparable performance to our advanced HV3S results, it is difficult to make a convincing case for deploying these emerging and expensive technologies over GaAs for power applications below 6 GHz.

Further reading

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About the author

David Fanning is a senior research scientist and program manager in TriQuint's research and development group. He has focused on developing and transferring high-voltage PHEMT processes to production. Edward Beam is a TriQuint fellow responsible for III-V material growth and characterization. Prior to joining TriQuint, he oversaw III-V material development at Texas Instruments' central research laboratory. Paul Saunier is a fellow at TriQuint Semiconductor responsible for the development of advanced GaN and GaAs devices. He is the principal investigator for the DARPA contract for wide-bandgap semiconductors for RF applications. Hua-Quen Tserng is a TriQuint fellow involved with the characterization and design of high-voltage PHEMTs, AlGaN/GaN HEMTs and MMICs. He has over 30 years experience in the design and characterization of solid-state microwave devices and circuits.