

Evaluating Device Reliability Using Wafer-level Methodology

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ABSTRACT:

This paper demonstrates the viability of wafer-level methods as a means of evaluating device reliability using special reliability test structures and process control monitors (PCM). The results presented illustrate how this methodology can be employed to rapidly and effectively assess the impact of process or material changes on over-all reliability. The wafer-level methodology provides a quick feedback loop for the manufacturing group enhancing their ability to continuously improve on their processes.

INTRODUCTION:

In the compound semiconductor manufacturing environment making changes to an existing process or material to further enhance the performance of devices is commonplace. This fluidity necessitates a methodology that quickly evaluates the effects of these changes on fundamental process reliability.

The method of wafer-level accelerated lifetesting allows reliability studies in a straightforward and efficient manner. It can be accomplished on individual devices on a single wafer or on multiple devices on entire wafers. The wafer-level aspect of stressing provides a spatial map of reliability for a wafer and a single wafer can provide enough samples. Without the need for hundreds of devices and long-term lifetesting at lower temperatures this technique allows for a rapid and efficient means of evaluating device reliability. Packaging considerations are eliminated by doing these studies on wafer. This makes it easier to observe devices and do root cause analysis of the failure mechanism.

The results from wafer-level lifetesting provide a first-hand look at the consequences a process or material change affects on the reliability of devices. Wafer-level studies augment existing HTOL procedures and protocols. Based on the results, a decision to expend additional resources to do complete reliability studies can be made.

THE NATURE OF WAFER-LEVEL RELIABILITY STUDIES

The wafer-level approach to reliability studies at TriQuint Semiconductor builds on an extensive history of reliability studies in general. A crucial aspect of utilizing wafer-level reliability studies is the ability to interpret the results against a well-defined baseline. The historical context is built on data obtained from more traditional methods such as HTOL. This knowledge helps define key elements of

wafer-level lifetesting among them selecting which parameters matter, what failure criteria is acceptable and what wafer-level stresses are appropriate for these studies.

Another aspect of the wafer-level methodology is the use of standard test vehicles. At TriQuint Semiconductor, the standard test vehicle includes a unique reliability test mask populated by proprietary test structures as well as process control monitor (PCM) structures. These test structures allow wider latitudes of flexibility and efficiency that is not possible when employing specific circuitry.

The wafer-level methodology is most powerful when evaluating a process or material change against an established standard. This entails a careful measurement of key device parameters before and after wafer-level stress, comparing any notable shifts between the experimental and control cells. In general, the method of wafer-level lifetesting is a measure of relative reliability between a new process or material system and an established process or material system.

METHODOLOGY:

Wafer reliability testing involves two types of aging. Wafer-Scale Reliability (WSR) refers to reliability testing performed simultaneously on all structures contained on a whole wafer. All structures of interest are measured before the stress and once again after the stress. WSR aging is particularly applicable for whole-wafer stresses such as autoclave and temperature cycling. Wafer-Level Reliability (WLR) refers to aging tests applied to one structure at a time. An individual structure is measured and stressed and re-measured. Then, the next structure can be measured under the same stress or with different stress, so that distribution parameters and/or acceleration factors can be determined, and spatially mapped, within an individual wafer. WLR aging is particularly applicable for metal or resistor electromigration evaluations and capacitor Time Dependent Dielectric Breakdown (TDDB) studies.

A. WAFER-SCALE BAKE

A first-pass evaluation of device reliability involves a simple wafer-bake of wafers at 275°C. Key device parameters such as pinch-off, channel current, gate diode turn-on, breakdown voltage and gate leakage current are measured prior to and after the bake. This is done on whole wafers containing numerous devices. The bake is done in an ambient-air oven for 168 hours. This temperature is designed to cause a 20% decrease in channel current in a MESFET device as determined in a previous study [1].

B. WAFER-SCALE AUTOCLAVE

Wafer-scale autoclave is a rudimentary evaluation of device moisture sensitivity. Following JEDEC Standard Number 22, Method A102, whole wafers are autoclaved at 121°C with 100% relative humidity for 96-hours. Like wafer bake, key device parameters are measured before and after moisture exposure.

C. WAFER-LEVEL ACCELERATED LIFETESTING

A more in-depth characterization of device reliability includes a determination of the activation energy of a device under test (DUT). In this study, this is determined by thermally stressing individual DUTs using a specially designed reliability test structure. The test structure includes an on-wafer heating element that surrounds the DUT. The heating element utilizes a thin film resistor (TFR). Using this test structure, heating is localized around the DUT.

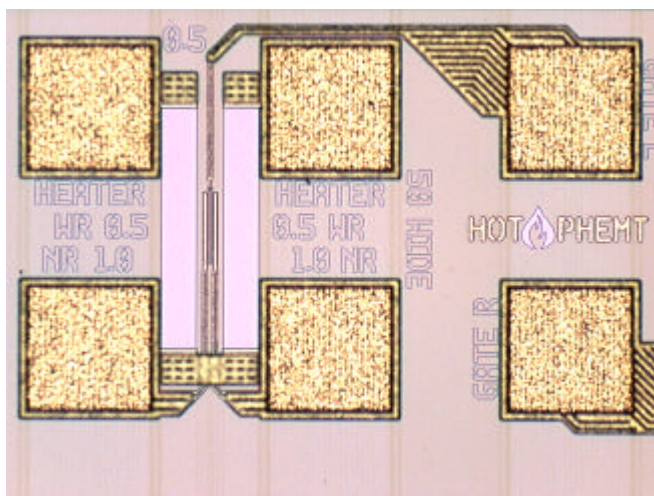


FIGURE 1. WAFER-LEVEL ACCELERATED LIFETEST STRUCTURE.

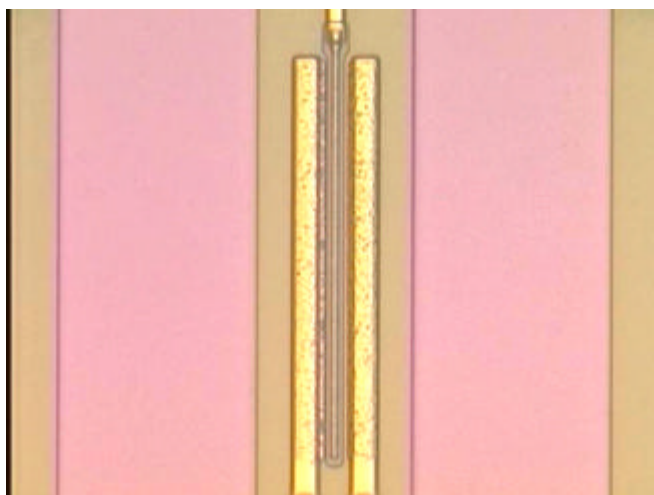


FIGURE 2. ON-WAFER HEATING ELEMENT AND DUT.

This allows different DUTs on the same wafer to be stressed at different temperatures. For the results presented in this paper, the DUT was a single-gate pHEMT device. But this methodology can be implemented for any given device of interest. Figure 1 shows the proprietary reliability test structure used in this study. The on-wafer test structure is a module in a broader reliability maskset. A single wafer can provide adequate test structures for the pHEMT device.

Prior to the HTOL studies, the temperature-power relationship of the heating element was characterized. By controlling the power across the heating element it is possible to stress individual devices at different temperatures. This heater also allows a feedback circuit to maintain a constant temperature around the device.

Key device parameters are measured at room temperature throughout the lifetesting. This allows a careful monitoring of the over-all health of the DUT.

RESULTS:

A. WAFER-SCALE BAKE

In pHEMT devices, gate-sinking is the predominant thermally-driven failure mechanism. The wafer-scale bake was employed as an early measure of device reliability on MOCVD-grown epitaxy material. Wafers from several vendors were compared to a wafer with the standard MBE-grown epitaxy. The results of the wafer bake are shown in first two figures (Figure 3 and Figure 4). The data for pinch-off voltage and saturated drain current indicates that at 275°C, none of the wafers exhibit the gate-sinking phenomena. These results indicate at first-glance device reliability of MOCVD-epitaxy material is no worse than of standard MBE-epitaxy starting material.

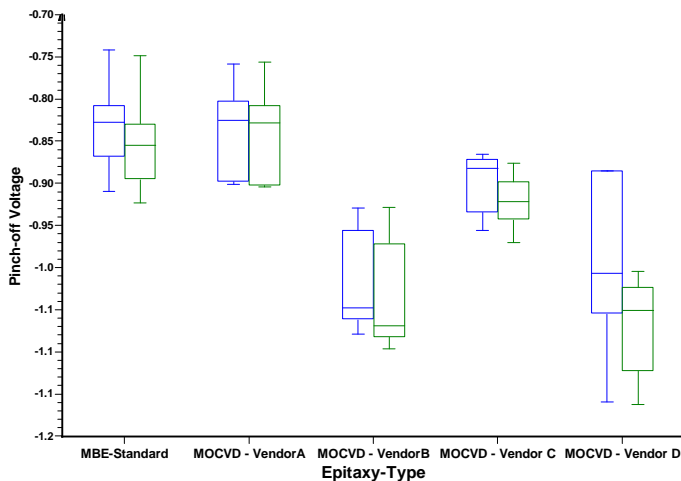


FIGURE 3. D-MODE PHEMT PINCH-OFF VOLTAGE (VP) BEFORE AND AFTER WAFER-BAKE (275°C)

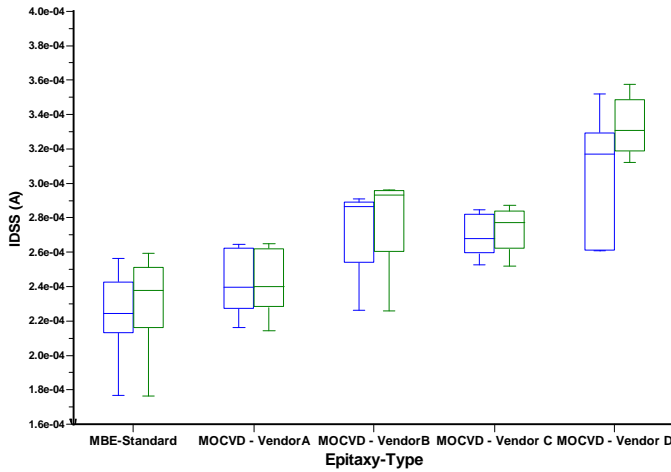


FIGURE 4. D-MODE pHEMT CHANNEL CURRENT (I_{DSS}) BEFORE AND AFTER WAFER-BAKE (275°C)

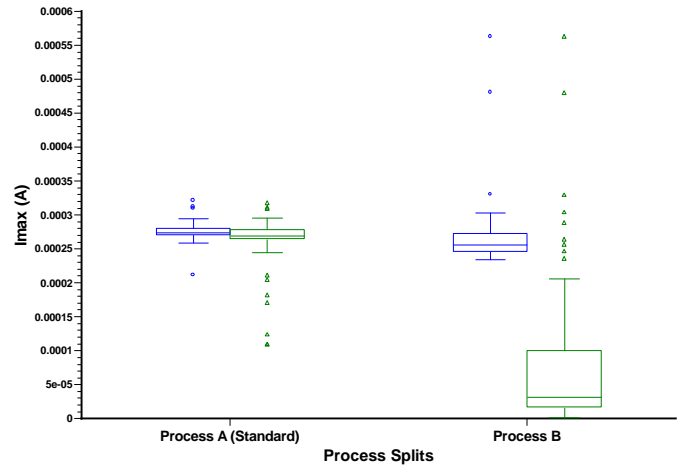


FIGURE 6. E-MODE pHEMT CHANNEL CURRENT (I_{MAX}) BEFORE AND AFTER AUTOCLAVE

B. WAFER-SCALE AUTOCLAVE

The moisture sensitivity of devices is not easily measurable. In this study, the reliability impact of a process change to device passivation was evaluated using wafer-scale autoclave. Figures 5 & 6 highlight the moisture robustness of the standard process. The data shows a significant degradation of pinch-off voltage and maximum drain current for the experimental cell compared to the standard process. The change to the device passivation in the experimental cell compromised the reliability of the pHEMT device.

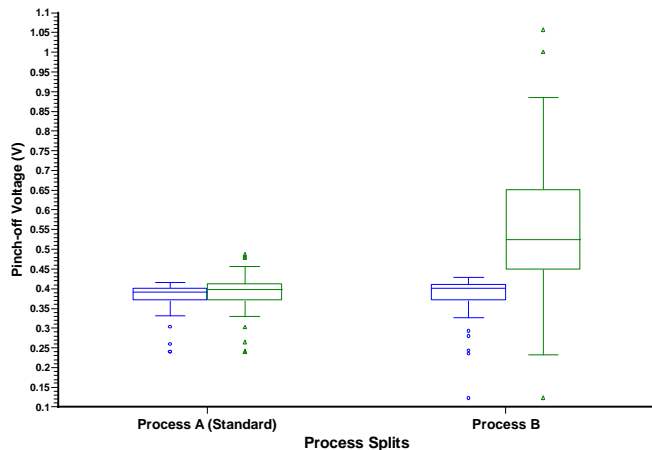


FIGURE 5. E-MODE pHEMT PINCH-OFF VOLTAGE (V_P) BEFORE AND AFTER AUTOCLAVE

C. WAFER-LEVEL ACCELERATED LIFETESTING

A preliminary assessment of parametric data collected showed a significant change in the measured drain current over a period of time. The decrease in drain current was observed on depletion-mode devices. To determine the activation energy associated with this failure mode a 10% decrease in drain current was set as the failure criteria for both pHEMT devices in line with current industry expectations.

Figure 7 shows the degradation of saturated drain current (I_{DSS}) at two different temperatures measured on the depletion-mode pHEMT device.

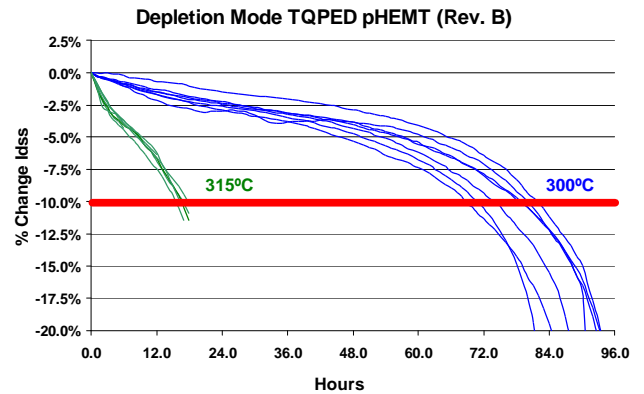


FIGURE 7. PARAMETRIC DEGRADATION AT TWO DIFFERENT AGING TEMPERATURES

The pHEMT devices were stressed at temperatures of 300°C and 315°C using the on-board heating element shown in Figure 1. Throughout the stress cycle, the drain current was monitored at fixed intervals at room temperature with no power applied to the heating element. During the measurement cycle, other device parameters besides the drain current are monitored. It took an average of 73.7 hours at 300°C to see a 10% reduction in the drain current of the depletion mode pHEMT device. At 315°C , it took an average of 17.5 hours to see the same effect.

Figure 8 shows the Arrhenius plot for the depletion-mode device. An activation energy of 2.77eV is calculated for this type of failure mechanism in the depletion-mode pHEMT [2].

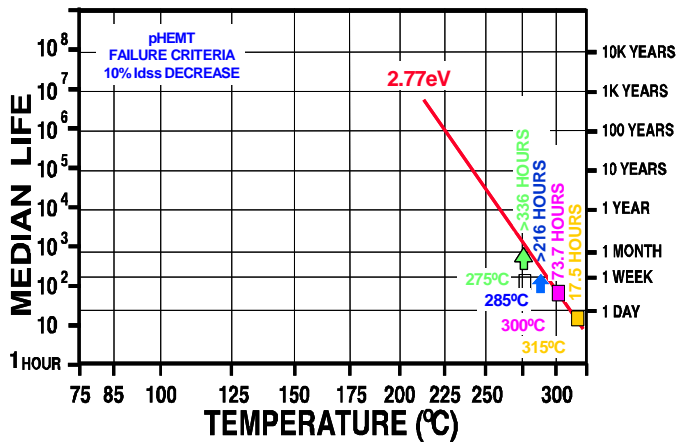


FIGURE 8. ARRHENIUS PLOT FOR THE TQPED DEPLETION-MODE PHEMT DEVICE.

Two points on an Arrhenius graph are sufficient to estimate the activation energy of a given failure mechanism. Additional points are, of course, more desirable in establishing the over-all shape of the curve. In addition to the data presented in this paper, supplementary points at 275°C and 285°C are referenced in the previous graphs. The transistors baked at these temperatures show no failures after 336 hours and 216 hours respectively for both depletion-mode and enhancement-mode pHEMT devices. These two additional data points point to a steeper slope of the temperature-median life curve as drawn.

Figure 9 shows the comparison between the activation energy of Triquint Semiconductor's TQPED and TQTRx process families. TQTRx is a MESFET process and the failure criterion is a 20% decrease in drain current [1].

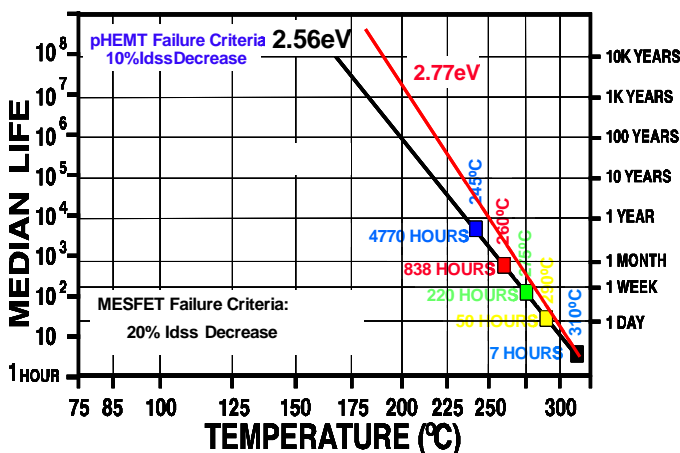


FIGURE 9. ARRHENIUS PLOT FOR THE TQTRx (MESFET) AND TQPED (PHEMT) PROCESS FAMILIES.

The resulting activation energies associated with a reduction in drain current derived from wafer-level accelerated lifestesting are comparable to ones obtained using more traditional HTOL methods. These results demonstrate that the on-wafer heating element adequately provides the necessary stress to thermally accelerate failure mechanisms. To further improve on the goodness of the results, additional data at other temperatures can be easily obtained using the on-board heater.

SUMMARY:

Wafer-level methods to evaluate device reliability are a viable alternative to more traditional HTOL studies. Reliability testing on wafers is a fast and efficient method of assessing device reliability. It works best in conjunction with an established baseline where expeditious comparisons are adequate enough to determine effects on over-all reliability.

The wafer-level technique makes it possible to sample multiple devices without the concerns for overhead and cycle time imposed by assembly and packaging. The methodology allows a greater degree of flexibility using a variety of temperatures and utilizing various bias conditions.

The wafer form remains intact during the reliability studies and a spatial variation of device reliability can be characterized at the same time.

The wafer-level methodology is thus ideal in a manufacturing environment where it is necessary to quickly evaluate how process improvements or material changes impact device degradation mechanisms and lifetimes. It is an important tool that augments more traditional HTOL methods.

REFERENCES:

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- [2] Hamada, Dorothy June M. and Roesch, William J. "Wafer-level Accelerated Life-testing of Individual Devices." I-2, Reliability Of Compound Semiconductor Workshop, Programs and Abstracts, October 2007.

ACRONYMS:

- DUT: Device Under Test
- HTOL: High Temperature Operating Lifestest
- MBE: Molecular Beam Epitaxy
- MOCVD: Metallo-Organic Chemical Vapor Deposition
- PCM: Process Control Monitor
- pHEMT: Pseudomorphic High Electron Mobility Transistor
- TDDDB: Time Dependent Dielectric Breakdown
- TFR: Thin Film Resistor
- WLR: Wafer-Level Reliability
- WSR: Wafer-Scale Reliability