

Impact of Electrical Degradation on Trapping Characteristics of GaN High Electron Mobility Transistors

Jungwoo Joh and Jesús A. del Alamo

Microsystems Technology Laboratories, MIT, Cambridge, MA 02139, USA, jungwoo@mit.edu

Abstract

One of the most deleterious effects of electrical degradation of GaN HEMTs is an increase in carrier trapping and subsequent current collapse. In this work, we have investigated the trapping and detrapping characteristics of GaN HEMTs before and after device degradation through a new current transient analysis methodology. We have found that electrical stress beyond a critical voltage significantly enhances trapping behavior inside the AlGaN barrier layer or at the surface. However, trapping in the buffer was found to be intact after device degradation.

Introduction

GaN high electron mobility transistors (HEMTs) have demonstrated outstanding performance in RF power and high voltage switching applications [1, 2]. Although the reliability of GaN HEMTs has been improving [3], these devices still suffer from a variety of degradation mechanisms [4-6]. One of the most deleterious effects of electrical degradation is an increase in carrier trapping and subsequent current collapse [4, 6-8]. To date, a detailed understanding of the nature, location and trapping/detrapping time constants of these traps is not available.

In this work, we have investigated the trapping and detrapping characteristics of GaN HEMTs before and after device degradation through a new current transient analysis methodology. In fresh devices, we can identify trapping occurring in the GaN buffer and also at the surface or inside the

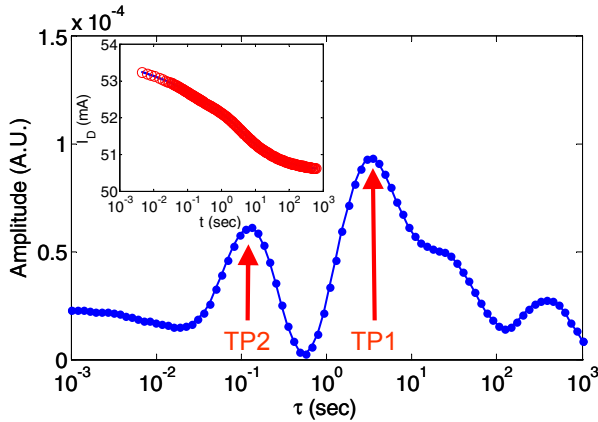


Fig 1. Trapping transient of I_D (inset) and time constant analysis of a fresh device in the ON state ($V_{GS}=1$ V, $V_{DS}=6$ V) at 30 C. No pulse was applied before the transient measurement. In the inset, the circled data points are measured I_D and solid line is the fitted curve. Two major trapping processes, TP1 and TP2, can be identified.

AlGaN barrier. We have also found that electrical degradation introduces new traps with a broad spectrum of detrapping time constants in the drain side of the device, either inside the AlGaN barrier layer or at the device surface. In contrast, buffer trapping is not affected by electrical degradation.

Experimental: Trapping and Detrapping in Fresh Device

We have studied $L_G=0.25$ μm millimeter-wave HEMTs with a source field plate [3]. The device width is 2×25 μm . Transient experiments in fresh and stressed devices were performed at temperatures between -60 to 130 C. After each experiment, the initial condition of the device was completely recovered by shining microscope light for 30 s. The trapping and detrapping processes were analyzed by least mean square fitting to a sum of pure exponentials, $I = \sum a_i \exp(-t/\tau_i) + c$. We have used 100 exponentials with time constants that are equally spaced logarithmically in time. Positive (negative) values of a_i correspond to trapping (detrapping) processes. Our analysis is carried out in the ms to 10^3 s range.

First we studied trapping in a fresh device. We biased the device in the ON-state ($V_{GS}=1$, $V_{DS}=2\sim 8$ V) while monitoring I_D . A typical I_D transient is shown in the inset of Fig 1. The corresponding time constant spectrum is also shown. Two major trapping processes, TP1 and TP2, can be identified. Through experiments at different temperatures, we have found that the time constant for TP1 is thermally activated, while that of TP2 is insensitive to temperature (Fig 2). A sim-

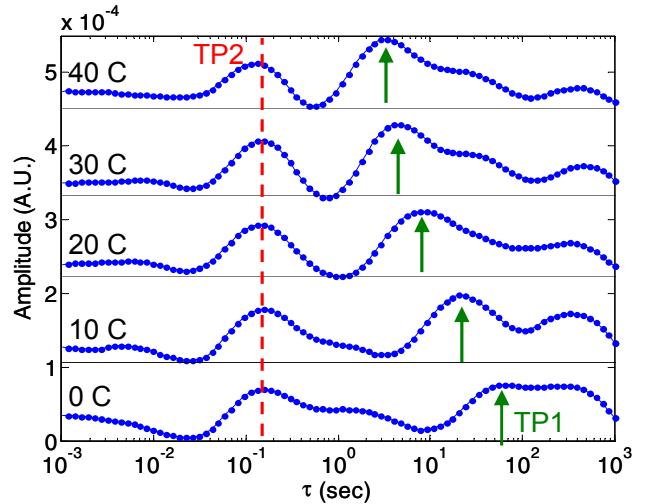


Fig 2. Time constant analysis for trapping transient in the ON-state (Fig 1) at different temperatures. The temperature was changed from 0 to 40 C. TP1 is affected by temperature, whereas TP2 is not.

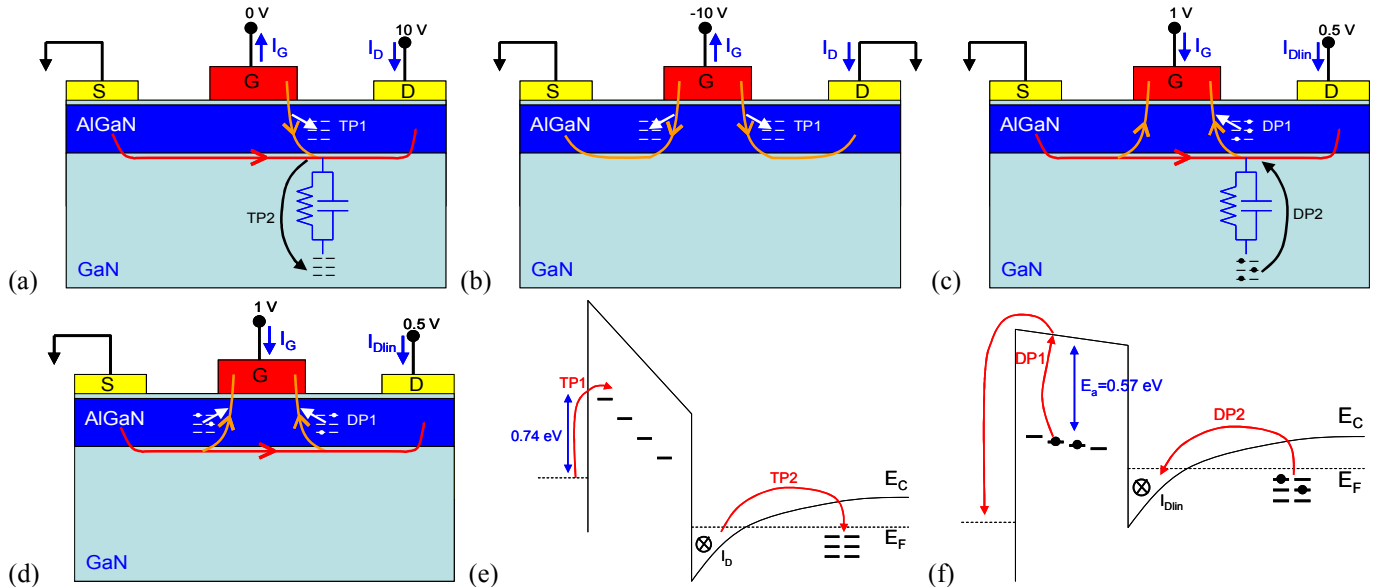


Fig 3. Different trapping and detrapping mechanisms. Arrows denote electron flow. (a) Trapping in the ON-state. (b) Trapping in the $V_{DS}=0$ state. (c) Detrapping after ON-state pulse. (d) Detrapping after $V_{DS}=0$ state pulse. (e) Band diagram for (a). (f) Band diagram for (c).

ilar trapping experiment was performed in the $V_{DS}=0$ state where device self heating is negligible. In this case, I_G is monitored over time. We observe a similar process to TP1 with $E_a=0.74$ eV at $V_{DG}=5$ V. In the $V_{DS}=0$ state, we do not observe a TP2-like process. From these and other experiments, we conclude that TP1 is associated with electron injection from the gate and trapping either inside the AlGaN barrier or at the surface (Fig 3a, b, and e). On the other hand, TP2 is related to trapping taking place in the channel or buffer (Fig 3a and e).

We also studied the recovery process from a current collapse event in a fresh device. Current collapse was induced by applying a voltage pulse of certain duration and monitoring the subsequent I_D transient. Although I_{Dmax} ($V_{GS}=2$, $V_{DS}=5$ V) can be a better parameter to monitor trapping behavior, in order to prevent trapping and self-heating that would take place during the measurement of I_{Dmax} transient, we have instead monitored I_{Dlin} ($V_{GS}=1$, $V_{DS}=0.5$ V). We

have experimentally confirmed that the transients of I_{Dmax} and I_{Dlin} are closely correlated. Fig 4 shows a detrapping transient of I_{Dlin} and the time constant analysis at -20 C after inducing current collapse through a 1 s long $V_{DS}=0$, $V_{GS}=-10$ V pulse. As one can see, there is a well defined recovery process, marked as DP1, with a time constant $\tau \sim 4$ s. This time constant is thermally activated with $E_a=0.57$ eV (Fig 5). A trap at this energy is widely seen in other DLTS or transient analyses [8, 9]. Since in the $V_{DS}=0$ condition we know that trapping only occurs in the AlGaN barrier or at the surface (Fig 3b), we can conclude that detrapping process DP1 is likely to be the reverse process of trapping process TP1 (Fig 3d) although there might be some trapping processes other than TP1 that are associated with DP1.

Current collapse after an ON-state pulse (1 s, $V_{GS}=0$ V, $V_{DS}=10$ V) with high I_D involves an additional detrapping

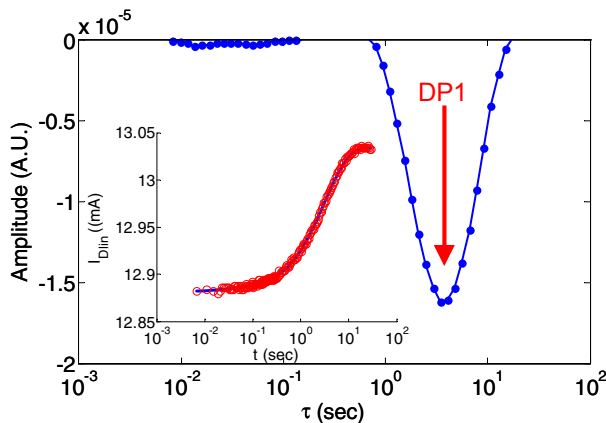


Fig 4. Time evolution of I_{Dlin} (inset) and time constant analysis at -20 C after applying a 1 s $V_{DS}=0$ and $V_{GS}=-10$ V pulse. The uncollapsed I_{Dlin} is 13.05 mA. This is the same fresh device as in Fig 1.

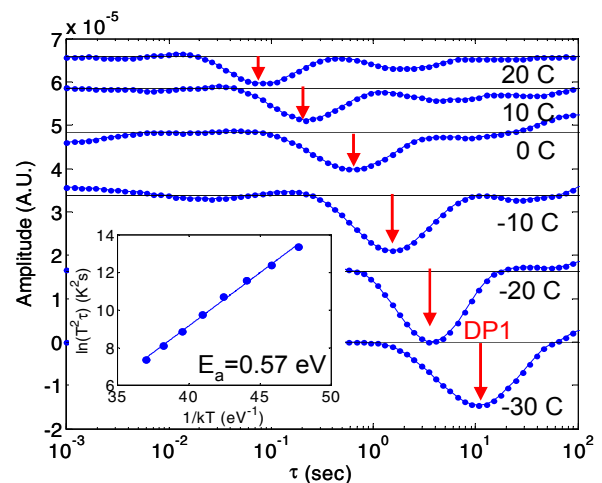


Fig 5. Time constant analysis of detrapping transient after a 1s $V_{DS}=0$ and $V_{GS}=-10$ V pulse for $T=-30$ to 20 C (inset: Time constant of DP1 as a function of temperature. $E_a=0.57$ eV).

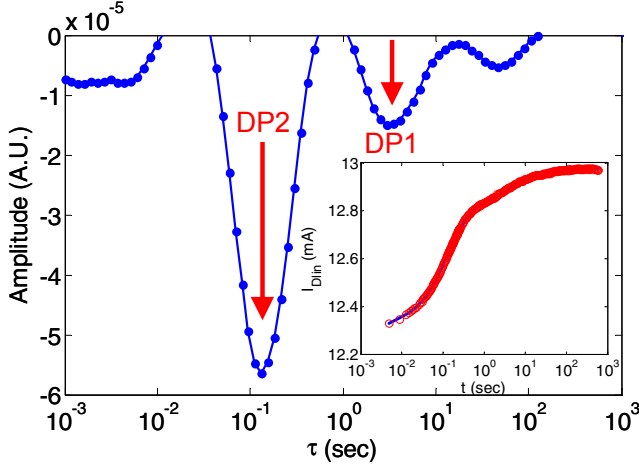


Fig 6. Time evolution of I_{Dlin} (inset) and time constant analysis at -20 C for 10 minutes after applying 1 second $V_{DS}=10$ and $V_{GS}=0$ V pulse. The same device (unstressed) was used as in Fig 1.

process, DP2, with time constant $\tau \sim 0.1$ s (Fig 6). Unlike DP1, the time constant of DP2 was found not to be thermally activated at all. This suggests that DP2 involves a bottleneck transport process in series with a detrapping process that is itself much faster than 0.1 s. DP2 was found to be negligible for an ON state pulse shorter than 0.1 s. Also, the magnitude of DP2 scales with the current level of the pulse. Interestingly, the time constant of DP2 is always exactly the same as that of TP2 observed in the ON-state trapping process. These results strongly suggest that DP2 and TP2 are both related to buffer trapping/detrapping of channel electrons (Fig 3a and c), and the time constant (~ 0.1 s) is the RC charging/discharging time [10]. In [11], current collapse due to high current and high V_{DS} pulse was ascribed to buffer trapping.

Effect of Electrical Degradation

We have also investigated the impact of electrical degradation on these trapping phenomena. A device was step stressed in the OFF state ($V_{GS}=-5$ V, $V_{DS}=5-48$ V in 1 V step,

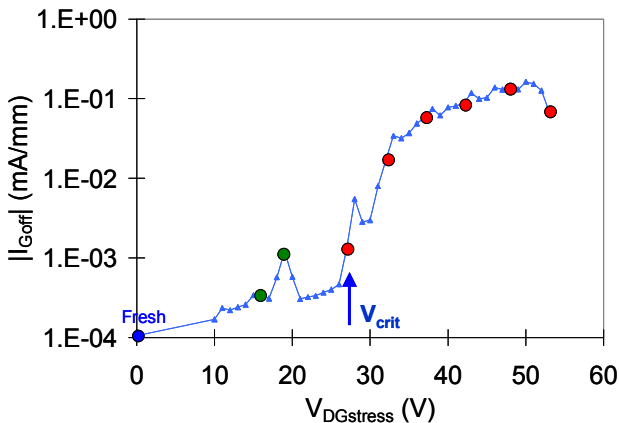


Fig 7. Change in I_{Goff} (I_G @ $V_{DS}=0.1$, $V_{GS}=-5$ V) in an OFF-state step stress ($V_{GS}=-5$, $V_{DS}=5-48$ V). The points when transient analyses were performed are marked with solid circles.

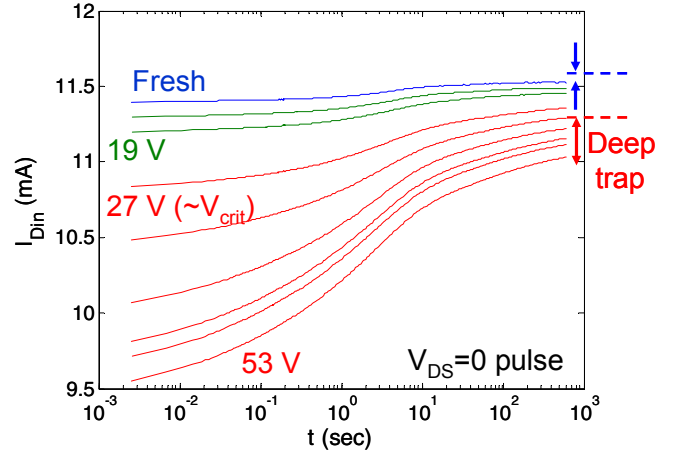


Fig 8. I_{Dlin} detrapping transient after current collapse introduced by a 1 s $V_{DS}=0$ and $V_{GS}=-10$ V pulse at -20 C. The uncollapsed levels of I_{Dlin} before and after the stress are marked with dashed lines. The transient characteristics were measured for the points marked with circles in Fig 7. Current collapse sharply increases beyond V_{crit} , and deep traps ($\tau > 1000$ s) are introduced after stressing.

1 min/step) at 100 C. The change in I_{Goff} is shown in Fig 7. As discussed in [12], I_{Goff} is a sensitive indicator of device degradation. It can be seen that I_{Goff} increases by 3 orders of magnitude beyond a critical voltage $V_{DGcrit} \sim 27$ V [5].

Trapping/detrapping analyses were performed before, during, and after the stress experiment. In Fig 8 and Fig 9, I_{Dlin} transient and time constant analysis after a $V_{DS}=0$ pulse are shown. Uncollapsed I_{Dlin} level (dashed lines on top right of Fig 8) decreased after stressing as a result of degradation that is not related to trapping. Current collapse and DP1 both increase sharply for stress beyond V_{crit} . Also, a broad spectrum of traps is introduced (Fig 9), and deep traps ($\tau > 1000$ s) are produced (marked with arrows in Fig 8). A similar trend is observed for detrapping after an ON-state pulse (Fig 10). However, unlike DP1, DP2 did not increase at all after stressing. This shows that no damage was introduced in the buffer layer. These results are summarized in Fig 11. A critical behavior is evident in the magnitude of DP1 and current col-

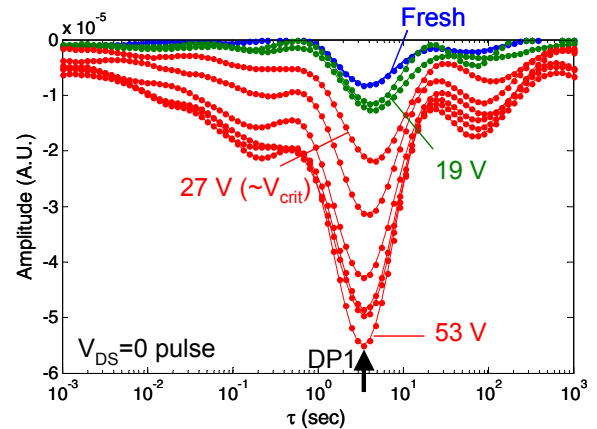


Fig 9. Time constant analysis of the data in Fig 8. DP1 shows a sharp increase beyond V_{crit} , and a broad spectrum of traps is introduced after stressing the device beyond the critical voltage.

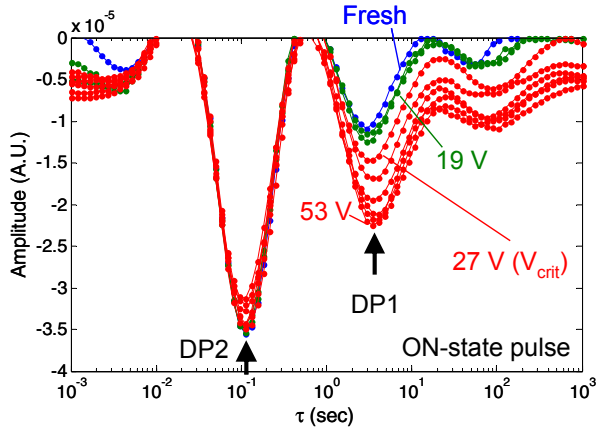


Fig 10. Time constant analysis of I_{Din} detrapping transient after current collapse introduced by a 1 s ON-state ($V_{DS}=10$ and $V_{GS}=0$ V) pulse at -20 C. The transient characteristics were measured for the points marked with circles in Fig 7. DP2 does not change, and a broad spectrum of long time constant traps are introduced beyond V_{crit} .

lapse.

In order to establish the location of the created traps, we measured the transient after an identical ON-state pulse with the source and the drain switched ($V_{SG}=10$ V, $V_{DG}=0$ V). In this case, a high electric field is applied in the source-gate region, and traps in that region are filled by the ON-state pulse. Since in this experiment $V_{DG}=0$, trapping is unlikely to occur in the drain side. As shown in Fig 12, we found that current collapse is about half and that deep trapping is about 1/7 compared to the normal measurement. This indicates that the source side of the device appears intact, and the generated traps are mostly localized in the gate to drain region. Fresh devices or devices that are symmetrically stressed in the $V_{DS}=0$ state do not show a significant difference when the source and the drain are exchanged. All of these results are consistent with our previous findings that the inverse piezoelectric effect introduces deep states by producing crystallographic defects under the high-field edge of the gate [4].

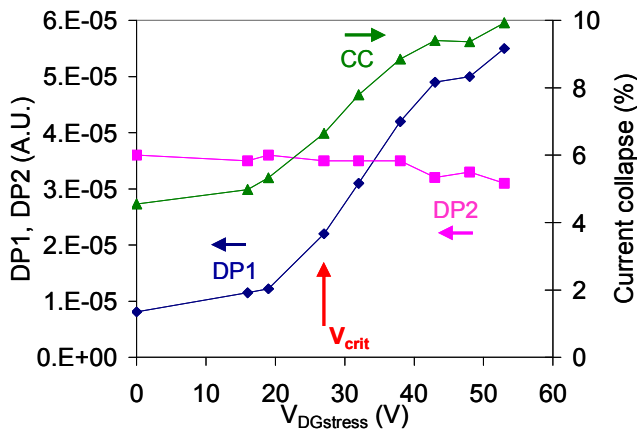


Fig 11. Change in DP1, DP2, and current collapse due to ON-state pulse as a function of the stress V_{DS} in the experiment of Fig 7. DP1 and current collapse increase sharply beyond V_{crit} , whereas DP2 does not change.

Conclusions

In summary, we have developed a simple methodology to investigate the characteristics of traps introduced during electrical degradation. In fresh devices, we identified several traps located above the channel, in the AlGaN or at the surface, and in the buffer. We found that after electrical degradation the concentration of traps above the channel increased in a marked way, and their energy spectrum broadened. These traps are generated beyond V_{crit} in the high field region of the device [5]. However, buffer trapping was unaffected by electrical stress. These results are consistent with previous findings that traps are produced in the AlGaN barrier layer through the inverse piezoelectric effect [4, 12]. Our methodology can be used for further understanding of trapping behavior and electrical degradation in GaN HEMTs.

Acknowledgements: This research has been funded by ARL under contract # W911QX-05-C-0087 (DARPA-WBGS program, Alfred Hung, contract monitor). We acknowledge collaboration with TriQuint Semiconductor and BAE Systems. This research has taken place in part at the Microsystems Technology Laboratories of MIT.

References

- [1] Y. Uemoto, *et al.*, *IEEE IEDM Tech. Digest*, pp. 861-864, 2007.
- [2] Y. F. Wu, *et al.*, *IEEE IEDM Tech. Digest*, pp. 405-407, 2007.
- [3] J. L. Jimenez, *et al.*, *IEEE Int. Rel. Phys. Symp. Proceedings*, 2008.
- [4] J. Joh, *et al.*, *IEEE IEDM Tech. Digest*, pp. 415-418, 2006.
- [5] J. Joh, *et al.*, *IEEE Electron Dev. Lett.*, vol. 29, pp. 287-289, 2008.
- [6] E. Zanoni, *et al.*, *IEEE IEDM Tech. Digest*, pp. 381-384, 2007.
- [7] J. A. Mittereder, *et al.*, *Appl. Phys. Lett.*, vol. 83, pp. 1650-1652, 2003.
- [8] A. Sozza, *et al.*, *IEEE IEDM Tech. Digest*, pp. 590-593, 2005.
- [9] T. Mizutani, *et al.*, *phys. stat. sol. (a)*, vol. 200, pp. 195-198, 2003.
- [10] E. Kohn, *et al.*, *IEEE Trans. MTTs*, vol. 51, pp. 634-642, 2003.
- [11] S. C. Binari, *et al.*, *Proc. IEEE*, vol. 90, pp. 1048-1058, 2002.
- [12] J. Joh, *et al.*, *IEEE IEDM Tech. Digest*, pp. 385-388, 2007.

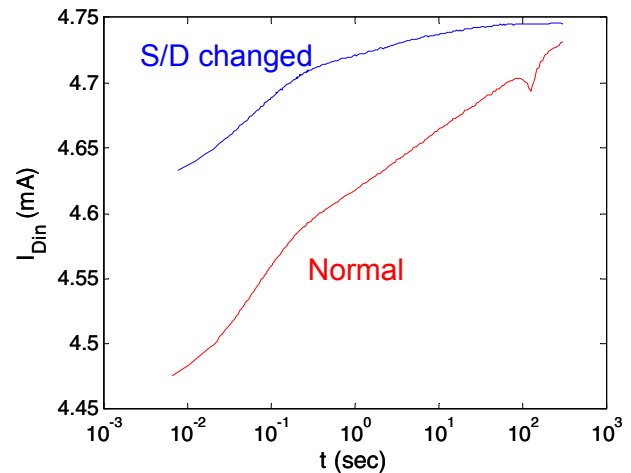


Fig 12. I_{Din} detrapping transient of a degraded device after current collapse introduced by 1 s $V_{DS}=10$ and $V_{GS}=0$ V (normal) and $V_{SD}=10$ and $V_{GD}=0$ V (S/D changed) pulses at 30 C. Half device (1 finger) was measured. The uncollapsed level of I_{Din} was 4.75 mA.