

A Wideband Power Amplifier MMIC Utilizing GaN on SiC HEMT Technology

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Abstract— The design and performance of a wideband power amplifier MMIC suitable for electronic warfare (EW) systems and other wide bandwidth applications is presented. The amplifier utilizes dual field plate 0.25- μm GaN on SiC device technology integrated into the three metal interconnect (3MI) process flow. Experimental results for the MMIC at 30V power supply operation demonstrate greater than 10 dB of small signal gain, 9W to 15W saturated output power and 20% to 38% peak power added efficiency over a 1.5GHz to 17GHz bandwidth.

I. INTRODUCTION

Modern electronic warfare systems specify amplifiers with high power, wide bandwidth and high efficiency. Until recently, solid state monolithic amplifier solutions have been capable of addressing this need for only modest output power levels. System designers have had to rely on TWT based power amplifiers to achieve order of magnitude increases in output power over available solid state devices. Wideband power amplifiers MMICs are also in demand for the test equipment market as well as general use.

To better serve these requirements researchers have developed power amplifier MMICs utilizing the nonuniform distributed power amplifier (NDPA) approach [1-4]. Impressive results have been published in both GaAs and GaN based semiconductor technologies. The achievable output power with the NDPA approach is proportional to V_d^2/R_L where V_d is the power supply voltage and R_L is the load impedance that the amplifier is driving. The output power of the amplifier may be increased by designing it to operate with a higher power supply voltage or to drive a lower load impedance.

If the power supply voltage is limited by the transistor technology being used then designing the NDPA for a lower load impedance is a viable option. Of course if the amplifier is ultimately to be operated in a 50 Ω system, impedance transforming networks will be required which may reduce the overall gain, bandwidth and output power of the circuit. A recent example of utilizing this approach was reported by Meharry, et al. [1]. The 2-stage power amplifier MMIC combines 4 NDPA stages designed to drive a 3 Ω load impedance with a wideband impedance transforming network that brought the output impedance back to 50 Ω . Measured

results under pulsed power conditions for the MMIC demonstrate 4W output power and 20% to 30% power added efficiency over a 4-18GHz bandwidth using a GaAs PHEMT process operated at 5V.

The other option for increasing output power is to use a high voltage transistor technology and a correspondingly higher power supply voltage. Modern GaN transistors are well suited for this application allowing a near order of magnitude increase in power supply voltage while simultaneously delivering similar gain and efficiency performance as GaAs PHEMT devices [5]. Recently, results for a wideband GaN NDPA MMIC were published by Gassmann, et. al. [2]. Measured continuous wave (CW) data for this MMIC demonstrate 5W to 7W output power and 19% to 32% PAE over a 2-15GHz bandwidth for 20V power supply operation.

In this paper the design and measured CW performance of a GaN on SiC NDPA MMIC covering a 1.5GHz to 17GHz frequency range is presented.

II. DEVICE TECHNOLOGY

The AlGaIn/GaN MMIC was fabricated entirely with the TriQuint Semiconductor baseline process on the 3-inch GaN on SiC manufacturing line.

The epitaxial structure has a Si GaN buffer with advanced Fe-doping for improved isolation. An AlN spacer was inserted between the buffer and the AlGaIn schottky barrier layer. The surface was terminated by a GaN cap layer for better leakage performance.

The active device epitaxial layers were isolated by performing mesa etch down to the GaN buffer. The ohmic source-drain spacing was 4- μm with nominal contact resistance of 0.5 Ω -mm. The contacts were formed by alloying a Ti/Al/Mo/Ti/Au metal stack at 850 $^\circ\text{C}$. The gate-length was defined by patterning and etching a 0.25- μm opening in the SiN_x. A second patterning and subsequent metallization over the etched SiN_x opening completes the gate metal and forms an integrated field-plate. In addition, a source-connected second field-plate (2FP) was implemented to reduce the high-field related device degradation. The distance from the source to the 2FP was selected to improve the PAE and gain at high voltage. For backside via, the SiC wafers were ground and polished to 100- μm , and the GaN/SiC vias were etched in an

ICP-RIE process. Finally, the backside ground plane was plated with $> 4\text{-}\mu\text{m}$ of Au.

The DC transfer characteristics are measured at $V_{DS} = 10\text{V}$ and $V_{GS} = -7\text{V}$ to 1.5V . Median threshold voltage was -4.2V with standard deviation of 0.35V across 4 wafers. The maximum dc transconductance was in excess of 300mS/mm . Maximum drain current at $V_{gs} = 1.5\text{V}$ was 1.07A/mm . The schottky forward turn-on voltage was 1.3V at 1mA/mm and reverse breakdown voltage was greater than 80V for $I_{GD} = 5\text{mA/mm}$.

Load pull data at 18GHz is plotted in Figure 1 for a $4 \times 100\mu\text{m}$ FET with a 40V drain bias. The results demonstrate greater than 50% PAE with an associated 6.2W/mm output power and 10dB power gain.

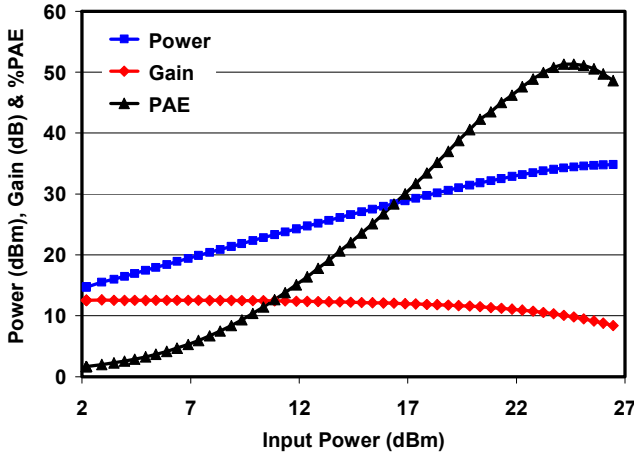


Figure 1. 18GHz Load pull results at 40V bias.

III. CIRCUIT DESIGN

As discussed in the introduction the NDPA topology was selected for this design. Theoretical details regarding this architecture are well described in the literature and will not be repeated here [3,4]. A simplified schematic diagram is shown in Figure 2.

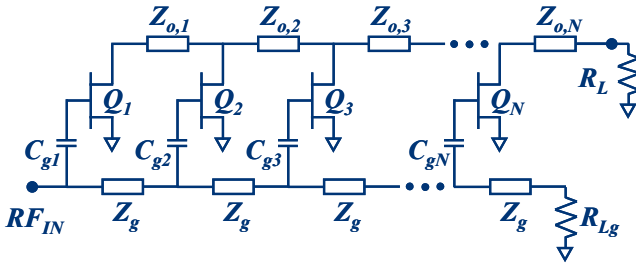


Figure 2. Basic NDPA topology.

The idea is to taper the drain line characteristic impedances, $Z_{o,n}$ to better maintain an optimum load for all of the FET cells. Under the following simplifying assumptions an approximate analysis of the circuit shown in Figure 2 can be performed. First, the transmission line lengths can be adjusted such that the FET currents add in-phase and second, the FET

output capacitance C_p can be absorbed into the transmission lines. At low frequencies the individual FET optimum load resistances, $R_{p,n}$ will combine in parallel and this parallel combination should be equal to the load impedance R_L to maximize the output power of the amplifier. In other words, given the normalized optimum load resistance the total FET periphery will be constrained by the following relation,

$$\frac{R_p (\Omega \cdot \text{mm})}{R_L} = \sum_{j=1}^N W_{Q_j} \quad (1)$$

Summing the currents at the drain node of each transistor produces the following recursive relationship for the line impedances,

$$Z_{o,n-1} \sum_{j=1}^{n-1} W_{Q_j} = Z_{o,n} \sum_{j=1}^n W_{Q_j} \quad (2)$$

where the characteristic impedance of the N th line will be equal to the load, $Z_{o,N} = R_L$. Therefore, for the $n=N$ case substituting (1) into (2) reveals that the right hand side of (2) is equal to the normalized optimum load resistance for the transistors. This can be shown to also be the case for arbitrary values of n and (2) simplifies to the following [4].

$$Z_{o,n} = R_p (\Omega \cdot \text{mm}) \left/ \sum_{j=1}^n W_{Q_j} \right. \quad (3)$$

Consider the 10 cell example shown in Table 1 where two different cases have been analyzed. The first case utilizes equal periphery FET cells and illustrates a fundamental problem. Due to the high voltage operation of GaN devices, FET cells typical of the frequency range of interest can easily have an R_p of several hundred Ohms. Unfortunately, it is difficult to realize microstrip transmission lines with characteristic impedances much greater than about 120Ω . The first transmission line for the equal cell size case is completely unrealizable.

NDPA Example	FET	Equal FET Sizes		Unequal FET Sizes	
FET R_p (Ohm-mm) = 120	Number	WG(mm)	Zo (Ohm)	WG(mm)	Zo (Ohm)
RL (Ohm) = 50	1	0.24	500	0.60	200
Total FET Width (mm) = 2.4	2	0.24	250	0.20	150
Number of Cells = 10	3	0.24	167	0.20	120
Supply Voltage (V) = 30	4	0.24	125	0.20	100
Max RF Power (W) = 9.0	5	0.24	100	0.20	86
	6	0.24	83	0.20	75
	7	0.24	71	0.20	67
	8	0.24	63	0.20	60
	9	0.24	56	0.20	55
	10	0.24	50	0.20	50

Table 1. 10 cell Non-Uniform Distributed PA example.

This transistor will be poorly loaded and will operate at reduced output power and efficiency. The situation can be improved by making the first FET cell larger than those that follow effectively limiting the maximum transmission line impedance in the circuit [4]. One can far better approximate

the characteristic impedance of the first transmission line for the unequal FET size case.

Typically NDPA designs utilize capacitors in series with the gate of each FET cell to increase the cut-off frequency of the composite gate transmission line at the expense of gain. The series capacitor values should also be tapered to equalize the RF drive voltage present at the gate of each transistor. A resistor will have to be placed in parallel with each gate capacitor to provide a gate bias path for the FETs.

A design goal for this MMIC was to achieve a 10:1 bandwidth including X-band and as much of Ku-band as possible. It was determined that a 10 cell design optimized the small signal gain over this frequency range. The first cell is sized at 520 μm with the remaining 9 cells sized at 320 μm each for a total periphery of 3.4mm. Circuit simulations were performed with AWR Microwave Office utilizing the nonlinear EEHEMT model fit to pulsed IV, small signal s-parameter and load pull data. The matching networks and drain bias circuits were determined by extensive EM simulation with the Sonnet EM software package. Circuits were fabricated with the TriQuint Semiconductor 3-metal interconnect (3MI) process which features high density capacitors (1200pF/mm²), thick plated lines (6.77 μm) and capacitors constructed directly over substrate vias. A photograph of the completed MMIC is shown in Figure 3, the circuit dimensions are 5.54mm x 2.77mm.

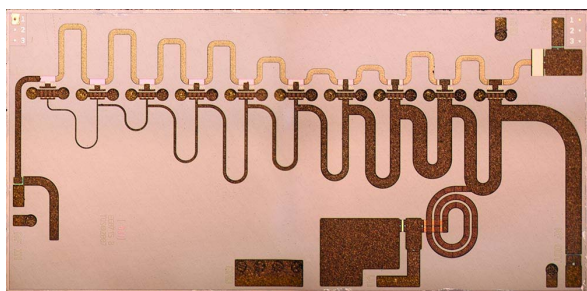


Figure 3. Photograph of the NDPA MMIC

IV. MEASURED RESULTS

Singulated, DC good MMICs were soldered to 40mil thick Cu-Moly carriers which were screwed down to an Aluminum test fixture with an intervening layer of Indium foil. Alumina 50 Ω de-embedding lines 470mil long were connected to the RF ports of the MMIC with two 25mil long bondwires. The far ends of the de-embedding lines were contacted with 2.9mm connectors which can be calibrated out of the measurements. A photograph of the test fixture is shown in Figure 4. The entire test fixture was mounted to an Aluminum heat sink with thermal grease. Temperature measurements of the carrier plate surface indicated that this arrangement maintained about a +30 $^{\circ}\text{C}$ base plate temperature for the MMIC.

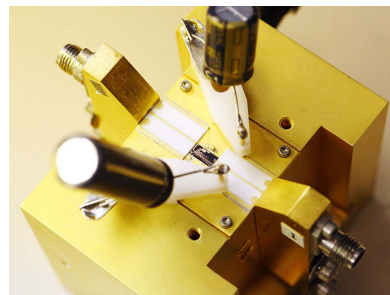


Figure 4. Test Fixture Assembly.

The amplifier MMICs were nominally biased at 30V and 200mA/mm current density. Measured results for the small signal gain and return loss are shown in Figure 5 for a sample of 8 amplifiers. The simulated small signal gain is shown as the broken line and is in good agreement with the measured results. The measured small signal gain is typically greater than 10dB from 1.5GHz to 17GHz.

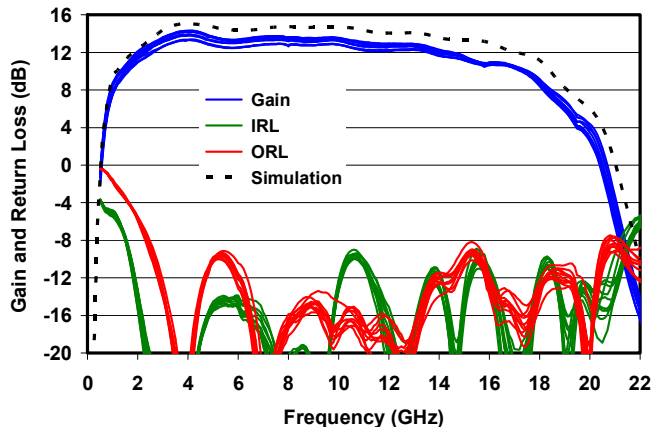


Figure 5. 30V Small signal gain and return loss.

Measured results for output power and efficiency with 32dBm CW input power are shown in Figure 6 for a sample of 6 amplifiers. The simulated results are shown as broken lines and are in reasonably good agreement with experiment. The discrepancy between the modeled and measured results for power and efficiency above 17GHz is under investigation. Possible causes are many including inaccuracies in the nonlinear model, harmonic terminations and coupling between the gate and drain lines. The output power is typically greater than 8W over a 1.5GHz to 17GHz frequency range with a peak value of 13W occurring at about 5GHz. The associated power added efficiency is typically greater than 20% with a maximum value of 38%. The power gain at 32dBm input power varies between about 7dB and 9dB. Power and efficiency data versus input power for one of the amplifiers is plotted in Figure 7 over a subset of frequencies. The observed compression curves are well behaved with no evidence of kink, odd-mode or driven oscillations. Saturated CW output power and peak power added efficiency for 30V, 35V and 40V power supply voltages are shown in Figure 8. In

general, increasing the supply voltage from 30V to 35V produces an increase in output power of 0.3dB to 0.5dB with a corresponding 2% point penalty in efficiency. Further increasing the supply voltage to 40V does little good and actually results in a reduction of output power at the upper end of the frequency band.

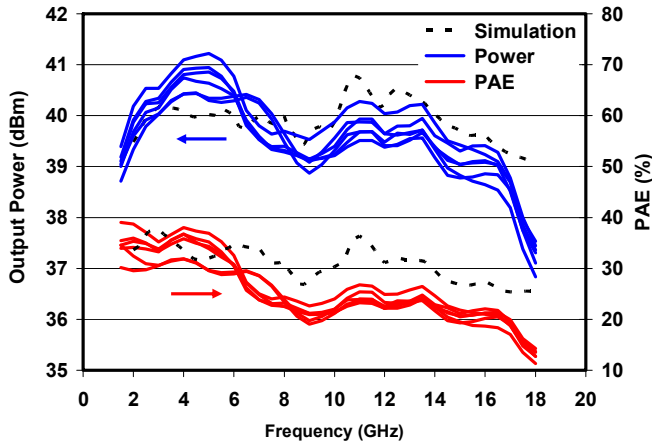


Figure 6. +30V CW power data at 32dBm input power.

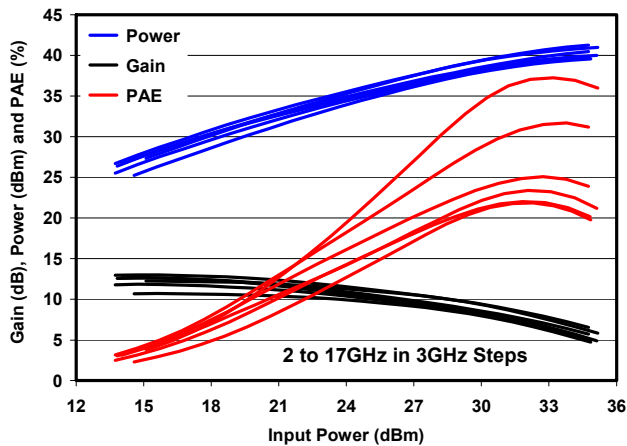


Figure 7. +30V CW power data vs. input power.

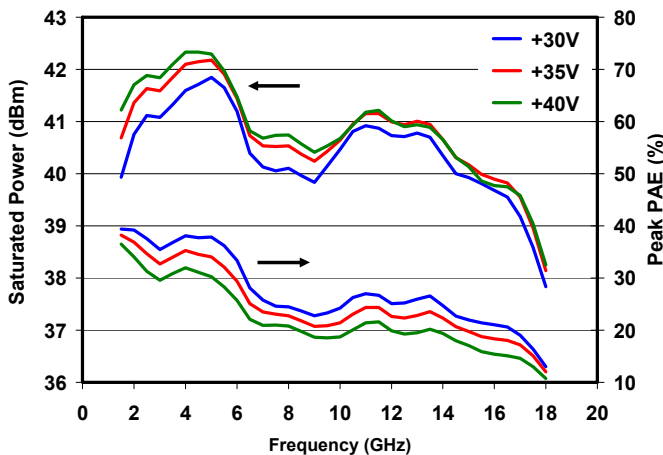


Figure 8. CW power data versus supply voltage

IV. CONCLUSIONS AND SUMMARY

The design and performance of a 1.5-17GHz nonuniform distributed power amplifier MMIC has been presented. The device utilizes 0.25 μ m dual field plate GaN on SiC transistor technology and was processed with the baseline TriQuint Semiconductor 3-metal interconnect flow. For the 1.5-17GHz band, experimental results demonstrate 9W to 15W saturated output power with an associated power added efficiency typically above 20%. To the authors knowledge these results are among the highest reported for a monolithic solid state power amplifier covering this frequency range.

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