Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors

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Abstract

In spite of their extraordinary performance, GaN HEMTs still lack solid reliability. Gate current degradation during RF power device operation is a great concern because it impacts PAE, gain, and output power. In this paper, we have experimentally studied gate current degradation under high forward and reverse bias conditions on the gate. We find that strong reverse bias on the gate produces defects that become paths for excess I_G. On the other hand, strong forward bias on the gate degrades Schottky junction probably due to thermal effects.

Introduction

GaN HEMTs exhibit great potential for high voltage switching and RF power applications. In spite of their extraordinary performance, these devices still lack solid reliability. In order to address this, a good understanding of the physical mechanisms behind device degradation is essential. Although a few reliability studies have been published, they have mostly focused on P_{out}, I_D, and R_D degradation [1-6]. However, gate current degradation is often also observed in stress tests [7] but has not received much attention. In RF power applications, gate current degradation is important because excessive gate current decreases PAE, gain, and output power.

In this paper, we study I_G degradation during electrical stress and show that for large reverse gate stress there is a sudden and irreversible increase in I_G of several orders of magnitude that occurs at a certain critical voltage. This increase in I_G is consistent with a defect formation mechanism through the inverse piezoelectric effect [4]. For large forward gate stress, there is also a strong increase in I_G but with a different pattern of degradation that suggests Schottky contact damage probably due to high current and high temperature.

Experimental

We have studied 0.25 um mmw experimental HEMTs with an integrated field plate. These devices are identical to those studied in [4]. For reverse gate stress, we have biased the devices in the V_{DS}=0 state and the OFF state in order to avoid self heating. Also, the impact of forward gate stress was investigated. During the stress tests, a number of figures of merit were extracted through a benign characterization suite. Among them, we have placed special attention on I_{Dmax} (I_D@V_{DS}=5 V, V_{GS}=2 V), R_D, R_S, and I_{Goff} (I_G@V_{DS}=0.1 V, V_{GS}=-5 V).

Fig 1 shows the result of a typical step-stress experiment in the V_{DS}=0 state. As we showed in [4], significant degradation in I_{Dmax}, R_S, and R_D suddenly occurs beyond a critical voltage V_{crit}. At this same V_{crit}, current collapse begins to increase [4]. Interestingly, as **Fig 1** reveals, there is also a sharp increase in $|I_{Goff}|$ at around V_{crit} where it often increases by several orders of magnitude.

Fig 2 shows V_{crit} for I_D and I_G degradation for several devices on the same wafer. V_{crit} for I_D was defined as V_{DG} at which I_{Dmax} becomes 95 % of its initial value, and V_{crit} for I_G was defined as V_{DG} at which a sharp increase in I_{Goff} occurs. This graph confirms that there is indeed a close correlation between the onset of I_D degradation reported in [4] and the sudden increase in I_G that is reported here. This close correlation suggests a common origin. Also of interest in **Fig 2** is to

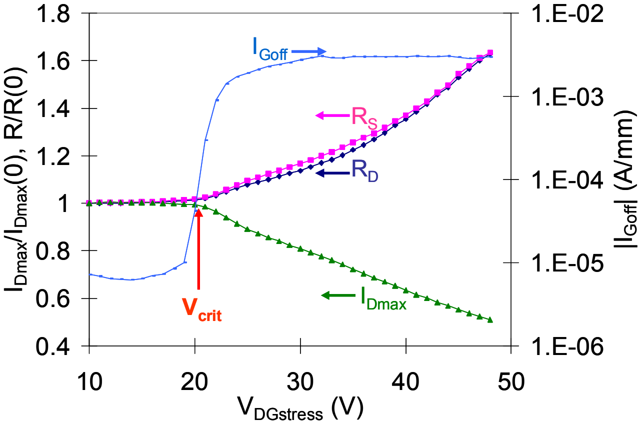

Fig 1. Change in I_{Dmax}, R_S, R_D, and I_{Goff} in a V_{DS}=0 step-stress experiment at room temperature. V_{GS} was stepped from -10 V to -50 V in 1 V steps (1 min/step).

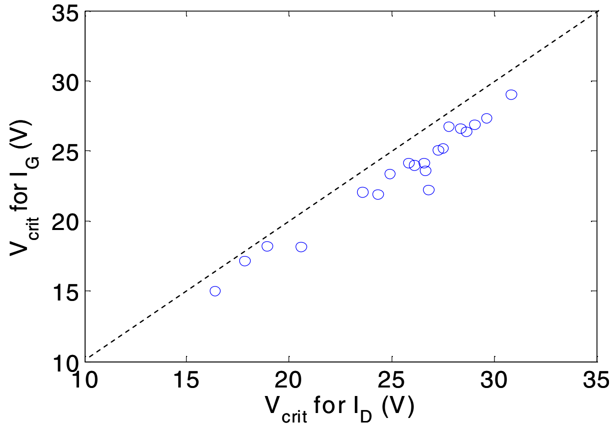

Fig 2. Correlation between critical voltage V_{crit} for I_D and I_G degradation. The devices were step-stressed in the V_{DS}=0 state from V_{GS}=-15 V to -45 V in 1 V steps (30 sec/step).

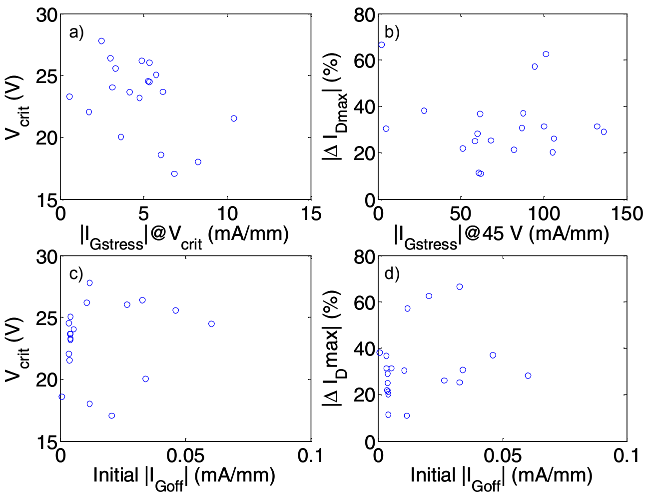

Fig 3. Correlation between gate current and degradation in V_{DS}=0 step-stress experiments of Fig 2: (a) V_{crit} and $I_{Gstress}$ at V_{crit}; (b) total I_{Dmax} reduction and $I_{Gstress}$ at 45 V; (c) V_{crit} and initial I_{Goff}; (d) I_{Dmax} degradation and initial I_{Goff}.

note the broad distribution in V_{crit} across a single wafer. We have observed this in other wafers with different device structures. This broad distribution implies a connection between degradation and some slow changing local wafer or epilayer attribute. In our experiments we consistently find that adjoining devices show very well matched values of V_{crit} with a difference that is typically smaller than 1 V.

While I_G and I_D degradation appear to be closely related, we do not find any causal relation between the two. There is no correlation between V_{crit} and the stress gate current at V_{crit} (**Fig 3a**), nor the total drain current loss after $V_{DGstress}$=45 V and the final stress gate current at this voltage (**Fig 3b**). Also, the initial gate current is not a predictor of degradation measured as V_{crit} (**Fig 3c**) or loss in I_{Dmax} (**Fig 3d**).

Fig 4 shows I_G-V_{GS} characteristics before and after the stress experiment of **Fig 1**. The reverse leakage current has increased and the forward turn-on voltage V_{Gon} has decreased, which suggests a lowering of the Schottky barrier height. In fact, the activation energy for I_{Goff} significantly decreased from 0.45 eV to 0.03 eV. However, the ideality factor in the forward branch (about 2) is relatively unchanged. In separate step-stress tests in the OFF state, we find that only the gate current flowing into the drain is enhanced, indicating that I_G degradation is associated with high fields at the gate edge.

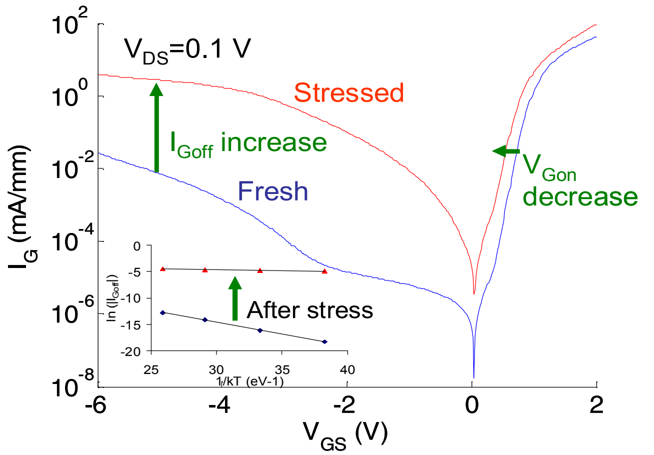

Fig 4. Change in the gate current at V_{DS}=0.1 V in the experiment of Fig 1. After the stress test, activation energy for I_{Goff} significantly decreased from 0.45 eV to 0.03 eV (inset).

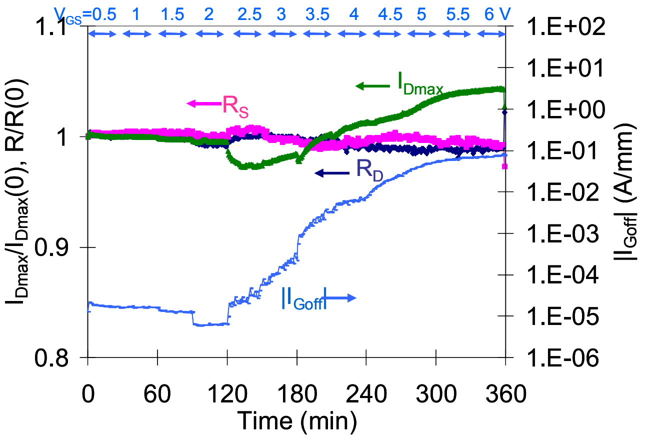

Fig 5. Change in I_{Dmax}, R_S, R_D, and I_{Goff} in a V_{DS}=0 step-stress experiments with positive gate bias. V_{GS} was stepped from 0.5 V to 6 V in 0.5 V steps. The device was stressed for 30 minutes at each step.

We have also investigated the effect of *positive* gate bias on I_G degradation. This is relevant in RF power applications as V_{GS} can swing rather positive under high input power drive. In a typical V_{DS}=0 experiment (**Fig 5**), we see that I_{Goff} increases at around V_{GS}=2.5 V ($I_{Gstress}$~180 mA/mm). Unlike for negative V_{GS} stress, in spite of the large stress gate current, there was negligible degradation in I_{Dmax}, R_D, and R_S, and we did not see an increase in current collapse. In addition, I_{Goff} degradation is rather gradual but reaching a value of 50 mA/mm at 5 V when $I_{Gstress}$ became 2 A/mm. It thus seems that the degradation mechanism in the forward gate regime is different from that in the reverse gate regime. A reduction in V_{Gon} along with ideality factor degradation (**Fig 6**) suggests that for high forward gate bias Schottky contact degrades severely due to the large gate current. After the degradation, the activation energy for I_{Goff} became essentially zero.

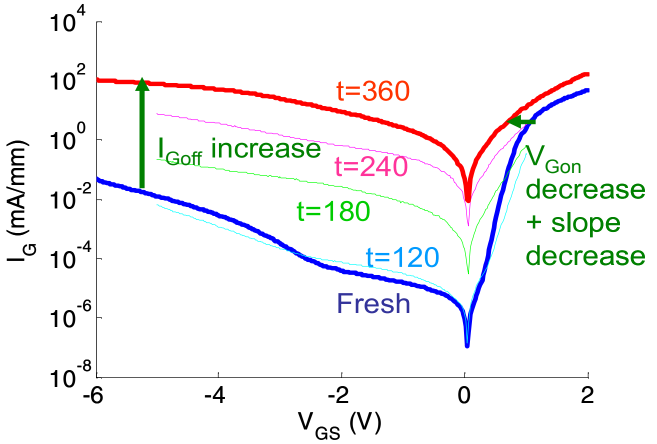

Fig 6. Change in the gate current at V_{DS}=0.1 V in the experiment of Fig 5. After degradation, activation energy for I_{Goff} became essentially zero, which suggests strong Ohmic behavior.

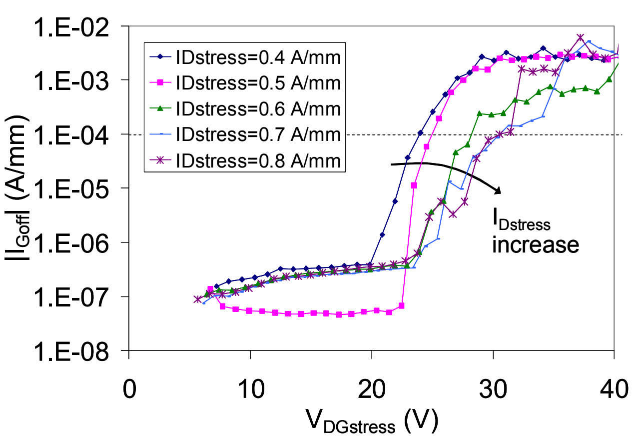

Fig 7. Change in $|I_{Goff}|$ in high-power step-stress experiments at different stress currents. V_{DS} was stepped from 5 to 40 V in 1 V step (1 min/step).

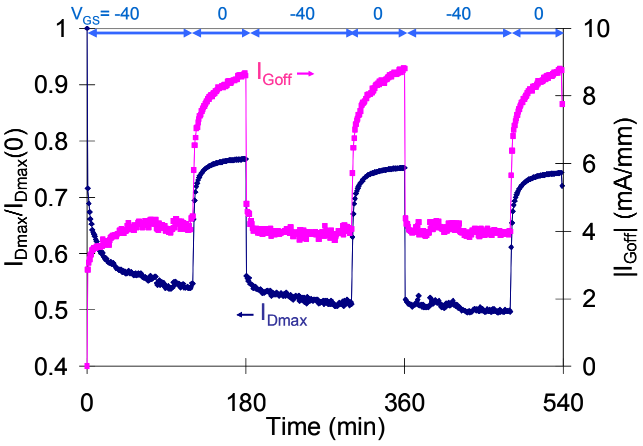

Fig 9. Change in I_{Dmax} and $|I_{Goff}|$ in a V_{DS}=0 stress-recovery experiment. The device was stressed at V_{GS}=-40 V for 120 minutes for the stress period followed by a 60 minutes recovery period. This cycle was repeated 3 times. When electrons are detrapped, I_{Goff} increases.

Discussion

A number of studies claim that hot electrons are behind the reliability problems of GaN HEMTs [1, 6]. In order to investigate the possible role of hot electrons on I_G degradation under large gate reverse bias in our devices, we have carried out step-stress experiments in the ON state with large current flow. We find that V_{crit} shows a *negative* dependence on stress current (**Fig 7**), which cannot be explained by a hot electron mechanism.

This and other experimental observations [4] are however consistent with a defect formation mechanism associated with excessive mechanical strain [4]. Under high V_{DG}, the high vertical electric field at the gate edge on the drain side introduces tensile strain in the AlGaN barrier due to the inverse piezoelectric effect. This adds on top of the tensile strain that is present in this layer due to the lattice mismatch with the GaN buffer. If the overall mechanical strain becomes excessive, crystallographic defects can be formed in the AlGaN barrier. These not only degrade I_D and R_D by trapping electrons but also aid electron tunneling between gate and channel through the AlGaN barrier, effectively lowering the Schottky barrier height of the gate (**Fig 8**).

The role of defects in I_G degradation can be readily observed in stress-recovery experiments. In these tests, a stress voltage is applied for a while followed by a period of recovery without bias [4]. This cycle is repeated several times. When the stress voltage is beyond the critical voltage, these kinds of experiments reveal strong trapping behavior in both I_D and I_G (**Fig 9**). Interestingly, in the recovery period when I_D increases, I_G also increases, and when stress is applied again, both I_D and I_G drop at the same time. These results make sense in the overall framework of our hypothesis in which trap formation and filling inside the AlGaN right next to the gate edge is responsible for I_D reduction. Those traps can participate in conduction between the gate and the channel but only if they are partially empty. This is enhanced during the recovery period.

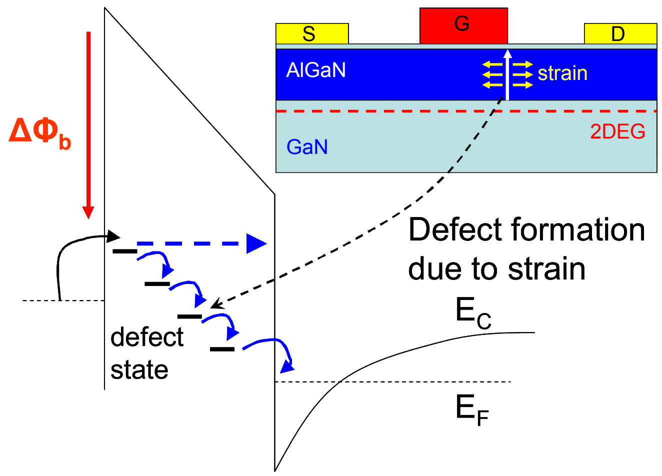

Fig 8. Conceptual I_G degradation mechanism for reverse bias stress. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path across the AlGaN barrier.

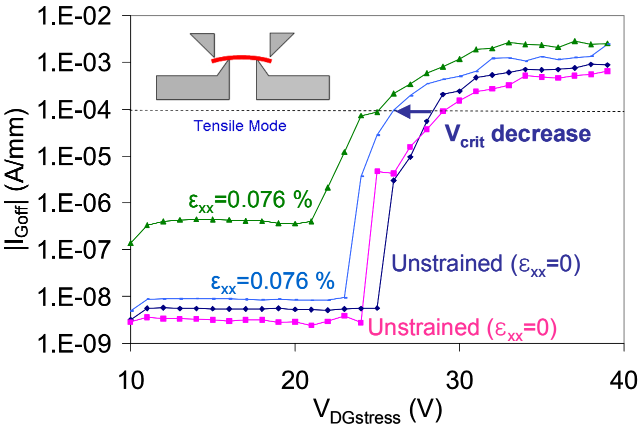

Fig 10. Change in I_{Goff} in V_{DS}=0 state step stress experiments. V_{GS} was stepped from -10 V to -40 V in a 1 V step (10 sec/step). V_{crit} is about 2 V lower for the devices that are stressed under 0.076% uniaxial mechanical strain. The introduced mechanical strain was separately calibrated through a laser reflection system.

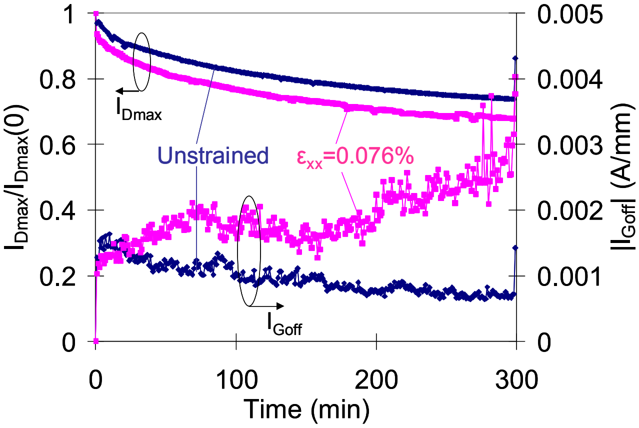

Fig 11. Change in I_{Dmax} and I_{Goff} of OFF-state stress experiments. The devices are stressed at V_{GS}=-7 V and V_{DS}=35 V. The device stressed under tensile mechanical strain shows larger degradation in both I_D and I_G.

At the heart of our hypothesis for I_D and I_G degradation is excessive mechanical stress in the AlGaN barrier. This can be tested through electrical stress experiments under tensile *mechanical* strain. In our model, additional tensile mechanical strain should enhance degradation since it adds on top of the initial tensile stress of the AlGaN barrier plus that introduced by the electric field through the inverse piezoelectric effect. In order to carry out this experiment, we have designed a jig through which we can apply uniaxial mechanical strain on a chip. We have verified that by itself, the level of strain applied does not damage the devices. At this time, when using small chips, our apparatus limits us to introducing tensile strain only.

Fig 10 shows change in I_{Goff} in typical V_{DS}=0 step-stress experiments under combined electrical and mechanical stress. Applying tensile strain of 0.076% reduces the critical voltage by about 2 V. We also observed a similar reduction of V_{crit} under mechanical strain in OFF-state step-stress experiments (not shown). In these experiments, we studied 5 pairs of identical devices that are located side by side on the same chip. In all cases the device under tensile mechanical strain exhibited a lower value of V_{crit} of around 1 to 3 V.

OFF-state stress experiments at constant electrical stress with and without additional mechanical strain also confirm that I_D and I_G degradation is enhanced by applying mechanical strain (**Fig 11**). OFF-state stress experiment in which the stress bias was fixed but the external mechanical strain was stepped up during the experiment (**Fig 12**) also revealed enhanced I_{Goff} degradation under increased mechanical strain.

All these experiments are consistent with our inverse piezoelectric effect hypothesis for electrical degradation of both I_G and I_D and are hard to explain through hot-electron type degradation mechanisms. The changes observed in V_{crit} upon the application of mechanical strain are small but systematic. The mechanical strain level that we are applying is about 30% of the strain induced by the peak electric field at around V_{crit} and about 8% of the critical strain for lattice relaxation. Under zero bias, we estimate that the initial mechanical strain of the AlGaN barrier in our devices is 77% of the critical strain (strain that yields a critical value of elastic energy). It is then reasonable that we are able to produce small but visible changes in V_{crit} upon the application of mechanical strain.

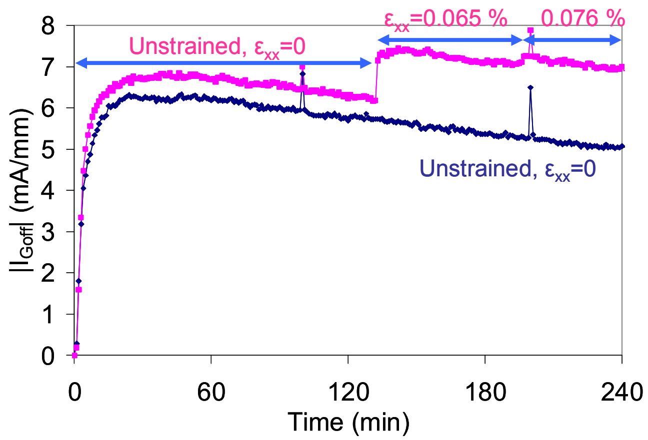

Fig 12. Time evolution of I_{Goff} in OFF-state stress experiments. Stress bias was V_{GS}=-7 V and V_{DS}=30 V. One device was stressed without mechanical strain. For the other device, uniaxial mechanical tensile strain ε_{xx}=0.065 and 0.076% was applied at t=133 and 197 min. Applying mechanical strain enhances I_G degradation.

Conclusions

In conclusion, we have found that the application of large positive gate bias degrades the Schottky contact of GaN HEMTs due to large current and/or high temperature. For high reverse gate bias, we find that I_G degradation occurs simultaneously to I_D degradation. Both appear to have a common origin in defect formation in the AlGaN barrier at the gate edge through the inverse piezoelectric effect [4]. These defects provide a leakage path for electrons and effectively lower the Schottky barrier height of the gate. In order to prevent this mode of I_G degradation, it is necessary to reduce the elastic energy and the vertical electric field in the AlGaN barrier.

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