Effects of RF stress on power and pulsed IV characteristics of AlGaN/GaN HEMTs with field-plate gates

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The effects of RF stress on power and pulsed IV characteristics of field-plated AlGaN/GaN HEMTs fabricated on two different epitaxial structures are presented. The power degradation characteristics are shown. The RF stress resulted in different degrees of RF voltage and current swing reduction on the two wafers. The current dispersion became more aggravated after RF stress under high quiescent drain bias conditions in one of the structures.

Introduction: AlGaN/GaN HEMTs have emerged as the most promising next generation devices for power amplifiers in the microwave and millimetre-wave frequency ranges. Several research groups have shown remarkable performance of 250 W on large gate-periphery devices [1] at S-band and 5.8 W at Ka-band [2], further demonstrating the potential of AlGaN/GaN-based devices. As the GaN-based HEMT technology transitions from research laboratories to products, reliability becomes one of the most important issues that need to be resolved. Several studies have reported the degradation characteristics of these devices after short-term DC and RF stress [3–6]. The post-stress characteristics of SiN_x-passivated conventional AlGaN/GaN HEMTs have shown reduction in transconductance, drain current and RF output power, and increase in gate leakage current. Severe current dispersion was also observed after stress on passivated devices, whereas no current dispersion was measured by pulsed IV prior to DC stress [5]. So far, there have been no reports on the effects of RF stress on AlGaN/GaN HEMTs with a field-plate (FP) gate. In this Letter, we present the effects of RF stress on current dispersion and power characteristics of FP AlGaN/GaN devices. The comparison of pulsed IV and RF power performance before and after RF stress of devices fabricated on two different epitaxial structures will be discussed.

Device fabrication and structure: The devices were fabricated with our AlGaN/GaN HEMT FP process. After isolation etch by BCl_3-based RIE and ohmic contacts formation by Ti/Al-based metallisation and alloy, the critical Si_3N_4 layer was deposited by plasma-enhanced chemical vapour deposition. Then, a 0.25 µm gate opening was etched through the Si_3N_4 layer using RIE etching. The FP gate was completed by defining a 1 µm pattern, centred with respect to the gate opening, and lifting-off gate metal. In this structure, a symmetrical gate metal overhang on top of the dielectric was created in the gate–source and gate–drain regions.

The epitaxial layers were MOCVD-grown on 6H-SiC substrates. Both AlGaN/GaN heterostructures were grown on ~1.5 µm of GaN buffer. Structure A has less than 150 Å of $Al_{0.3}Ga_{0.7}N$ barrier, while structure B has a barrier thickness of 260 Å. In addition, structure A has a very thin layer of 10 Å of GaN layer to cap off the $Al_{0.3}Ga_{0.7}N$ barrier. To enhance mobility and sheet charge density [7], a 10 Å thick AlN layer was inserted into both structures A and B. The sheet resistance is 270 and 287 Ω mm for structures A and B, respectively.

Results: RF stress tests were performed on 200 µm devices on both wafers, which were biased under class AB condition at $V_{DS} = 30$ or 40 V. The load and source impedances were tuned for maximum output power (P_{out}) at peak power added efficiency (PAE) in CW mode at 10 GHz. For each stress test, the device was stressed at the input power, for which the gain compression is about 3 dB. The degradation of P_{out} after an initial burn-in is shown in Fig. 1. At $V_{DS} = 30$ V, power degraded gradually and dropped by 0.14 dB after 50 h of stress for the device on structure A with an initial power performance of 7 W/mm, 43% PAE and 9.6 dB associated gain. When the RF stressed test ended at 90 h, P_{out} reduced by 0.22 dB for the device on structure A. In comparison, the device on structure B degraded sharply and produced a ΔP_{out} of −1 dB after 50 h of stress at 30 V drain bias with an initial power performance of 7.9 W/mm, 50% PAE and 9.3 dB associated gain. To investigate the drain-bias dependence, another device on structure A was subjected to RF stress at 40 V; it yielded a similar trend in ΔP_{out} compared with the device stressed at 30 V, as shown in Fig. 1. The results show that the devices on structure A are more stable under continuous RF bias.

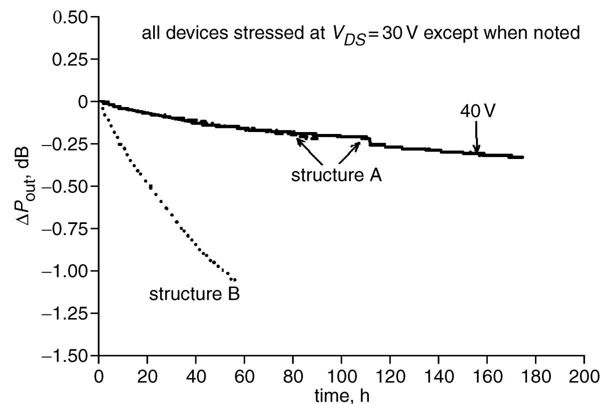

Fig. 1 *Degradation characteristics of output power under RF stress of AlGaN/GaN HEMTs with field-plate gates*

Load-pull power sweeps were measured before and after RF stress. Table 1 summarises the impact of RF stress on the power performance, including shift in peak RF voltage (V_p), RF knee voltage (V_k) and RF current calculated from the load impedance of the load-pull results. On both structures, a decrease in peak RF voltage and an increase in RF knee voltage, as well as the reduction in RF current, were observed after RF stress. The stress caused appreciable loss in P_{out} and PAE due to a large 6.3 V increase in V_k and 32 mA drop in peak RF current for the device on structure B. In contrast, the change in RF knee voltage and current swing induced by stress were considerably smaller for the devices on structure A at both 30 and 40 V.

Table 1: Summary of effects on power characteristics by RF stress of AlGaN/GaN HEMTs with field-plate gates

Structure	V_{Ds}	Condition	P_{out}	Gain	PAE	DE	V_{peak}	V_{knee}	$I_{d,peak}$	I_{DS}
	V		W/mm	dB	%	%	V	V	mA	mA
A	30	Before	7.20	8.88	44.0	50.6	26.8	3.2	107.5	94.9
	30	After	6.34	9.28	43.4	49.2	25.1	4.9	101.0	85.9
A	40	Before	9.14	9.86	39.8	44.4	30.2	9.8	121.0	103.0
	40	After	7.85	9.68	38.0	42.5	28.0	12.0	112.0	92.3
B	30	Before	7.64	6.79	49.5	62.8	24.7	5.3	123.6	81.1
	30	After	4.23	4.20	24.9	40.4	18.4	11.6	91.9	69.7

The dependence of current dispersion on RF stress of these devices with field-plate gates was measured with an Accent DIVA dynamic *I-V* analyser. The drain current is measured by pulsing from a quiescent bias point ($V_{DS,Q}$ and $V_{GS,Q}$) to each defined point in the *I–V* plane. In this work, a collapse factor, as illustrated in the inset of Fig. 2, is defined as the percentage change of pulsed I_{DS} ($V_{DS,Q}$ and $V_{GS,Q}$) from I_{DS}(DC) at $V_{DS} = 12$ V and $V_{GS} = 0$ V to quantify the degree of dispersion. The quiescent gate bias is fixed at pinch-off to simulate surface effects, while the quiescent drain bias was varied. Fig. 2 shows that, on both structures, the pulsed I_{DS} from $V_{GS,Q}$ = pinch-off and low field ($V_{DS,Q} = 10$ V) did not deviate from the DC drain current before any RF stress. This indicates that, at low field, our field-plate structure suppressed gate lag phenomenon related to the surface traps. As the quiescent drain bias was increased to higher voltages, the collapse factor remained constant for $V_{DS,Q}$ as high as 40 V on structure A, but it increased to 20% at $V_{DS,Q}$ of 30 V for structure B prior to stress. After RF stress, almost no changes were observed in the current collapse factor for structure A. For structure B, the collapse factor increased to 40% when pulsing at low field, deviating from the pre-stress value. When the same device was pulsed from 30 V, pulsed drain current was 50% less than the DC current, correlating to strong dispersion after RF stress. The effects on current dispersion after RF stress on both wafers correspond to the increase in RF V_k and reduction in I_{DS} from load-pull analysis.

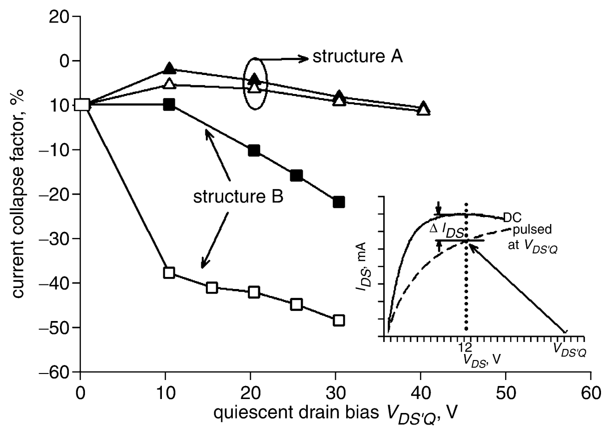

Fig. 2 *Current collapse factor, % change in pulsed drain current from the DC current, against quiescent drain bias before and after RF stress*

Inset: Illustration of measurement of current collapse factor
Solid symbols: before RF stress
Open symbols: after RF stress

Conclusions: We have presented the effect of RF stress on power and pulsed *I–V* characteristics on field-plated AlGaN/GaN HEMTs fabricated on two epitaxial structures. The RF stress resulted in a reduction in the RF voltage and current swing and caused severe current dispersion under high quiescent drain current conditions in one of the structures. Results of this study indicate that reliability of AlGaN/GaN HEMTs can potentially be improved by a combination of optimal epi design and field-plate process.

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