

# *TriQuint* <sup>®</sup> *SEMICONDUCTOR*

**TGA4953-SL and TGA4954-SL**  
**Optical Performance**  
**Using RZ Modulation**

April, 2009

# Outline

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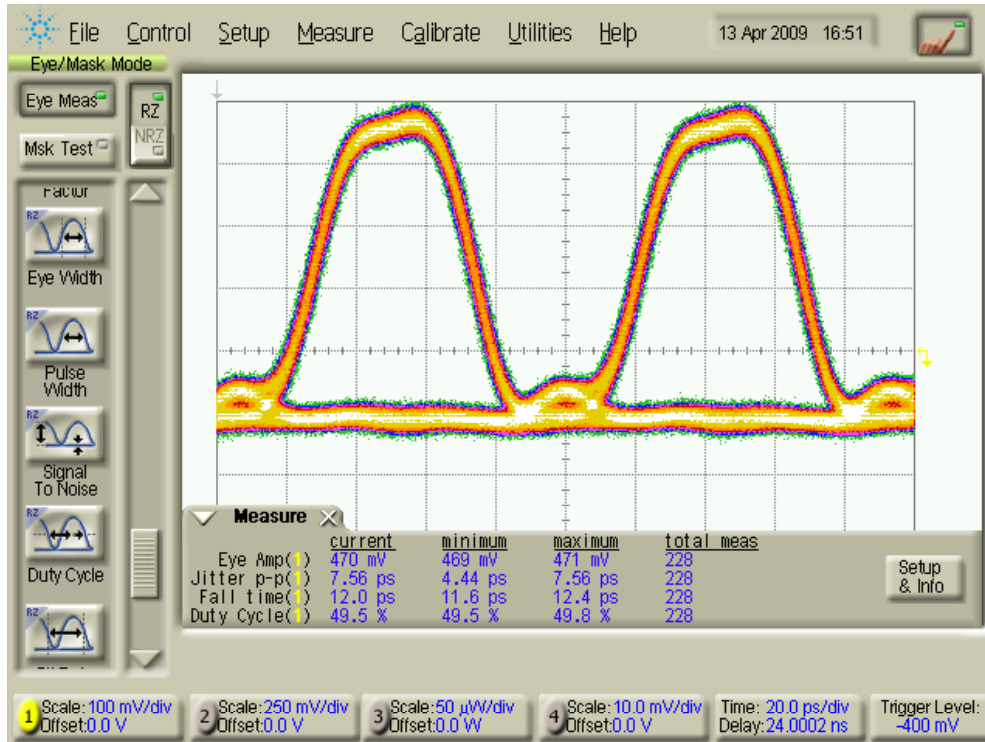
- **Introduction**
- **Input Eye**
- **TGA4954-SL Output Eye**
- **Optical performance using RZ modulation**
  1. **Experiment varying  $V_{c2}$ ,  $V_{g2}$ ,  $V_{c1}$ ,  $V_{g1}$  for  $V_{out} = 5.5V_{pp}$  and 50% Duty Cycle initial conditions (10.7 Gbps,  $V_{in} = 470 mV_{pp}$  @ 50% Duty Cycle)**
  2. **Obtain  $V_{out} = 5.5V_{pp}$  @ 50% Duty Cycle with minimum  $P_{diss}$**
  3. **Obtain max  $V_{out}$  at  $V_d = 5 V$**

# Introduction

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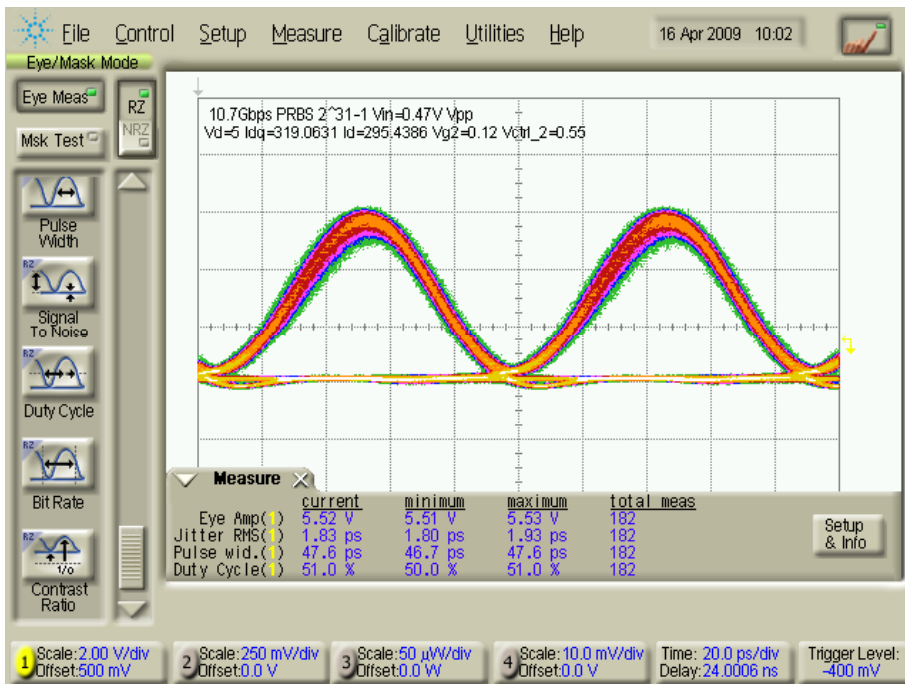
- **TGA4954-SL Evaluation boards tested using RZ (Return to Zero) Modulation**
- **Tests performed at room temperature using Anritsu MP1800A pulse pattern generator and an NRZ to RZ converter. Results monitored using Agilent Infiniium DCA 86100A Wide-Band Oscilloscope.**
- **No filter was inserted between the source and the DUT**
- **The purpose of these experiments was to show general trends in performance using RZ modulation. Although the TGA4954-SL evaluation board was used for these tests, the same trends should and can be applied to the TGA4953-SL.**

# Input Eye



- Data Rate = 10.7 Gbps
- Vout = 0.47 Vpp
- Duty Cycle = 50%
- PRBS  $2^{31} - 1$
- RZ signal generated from NRZ using separate converter

# Output Eye: $V_{out} = 5.5 \text{ Vpp}$



- Data Rate = 10.7 Gbps
- $V_{in} = 0.47 \text{ Vpp}$
- $V_{out} = 5.5 \text{ V}$
- Duty Cycle = 50%
- Eye S/N = 12.5
- Rise, Fall T = 23, 19 ps
- **$P_{diss} = 1.26 \text{ W}$**

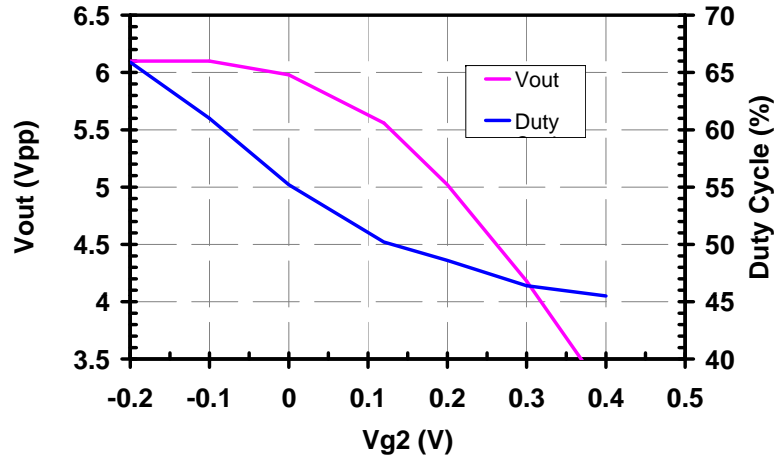
## Initial Bias Conditions:

$V_d = 5 \text{ V}$ ,  $I_{dq} = 334 \text{ mA}$ ,  $V_{g1} = -0.76 \text{ V}$ ,  $V_{g2} = +0.12 \text{ V}$ ,  $V_{c1} = 1 \text{ V}$ ,  $V_{c2} = 0.55 \text{ V}$ ,

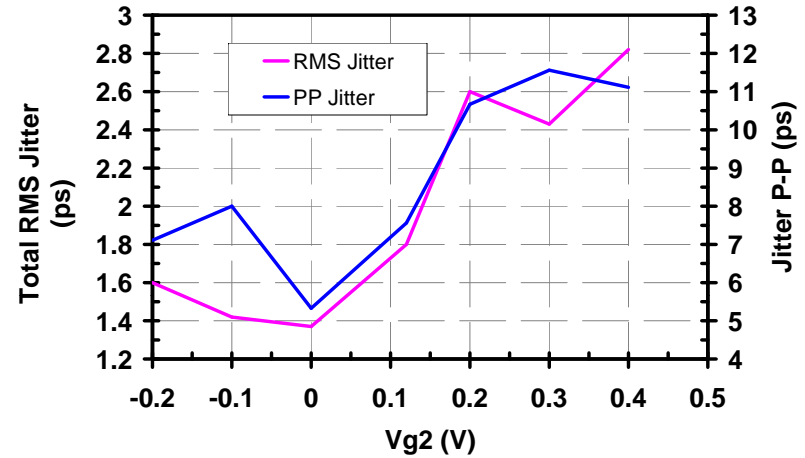
# Vary $V_{g2}$ from initial conditions:

$V_d = 5V$ ,  $V_{g1} = -0.76 V$ , Vary  $V_{g2}$ ,  $V_{c1} = 1.0 V$ ,  $V_{c2} = 0.55 V$

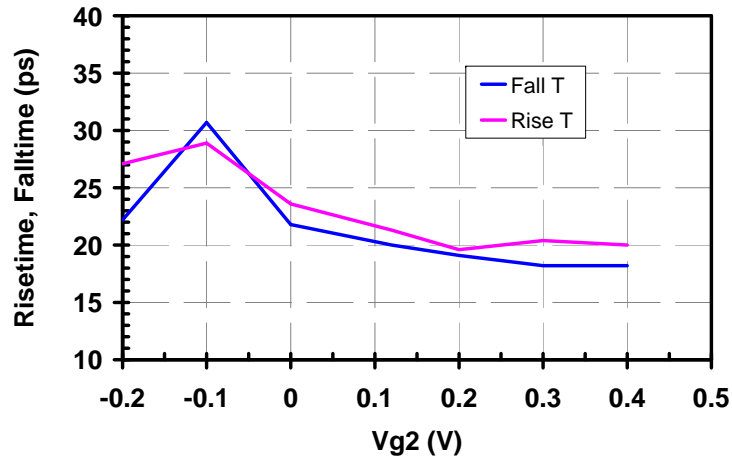
TGA4954-SL SN0635-001, 10.7 Gbps, 2<sup>31</sup>-1 PRBS, RZ Input  
 $V_{in} = 470 \text{ mVpp}$ , 10.7 Gbps,  $V_d = 5V$ ,  $V_{c1}=1V$ ,  $V_{g1}=-0.76V$ ,  $V_{c2}=0.55V$



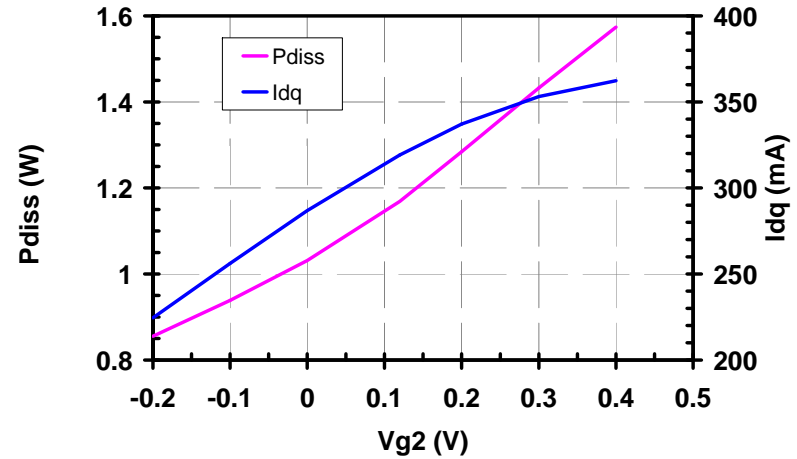
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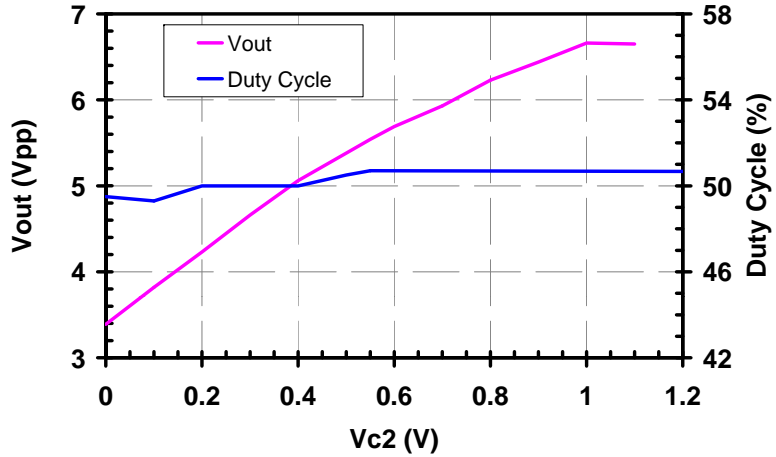
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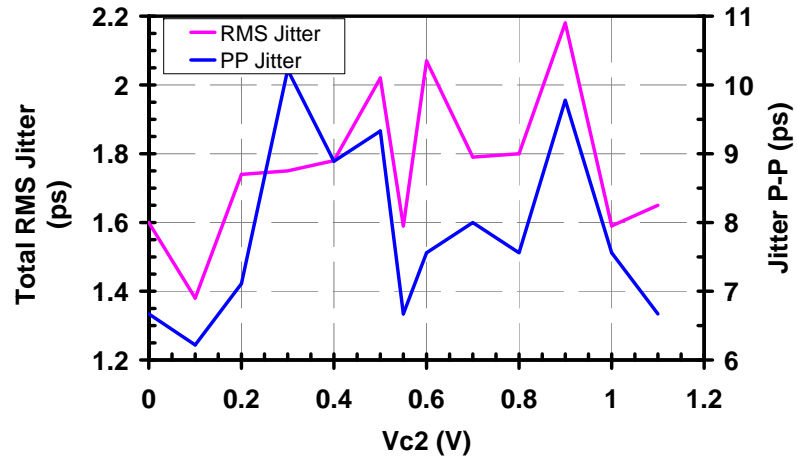
# Vary **Vc2** from initial conditions:

**Vd = 5V, Vg1 = -0.76 V, Vg2 = 0.12 V, Vc1 = 1.0 V, Vary Vc2**

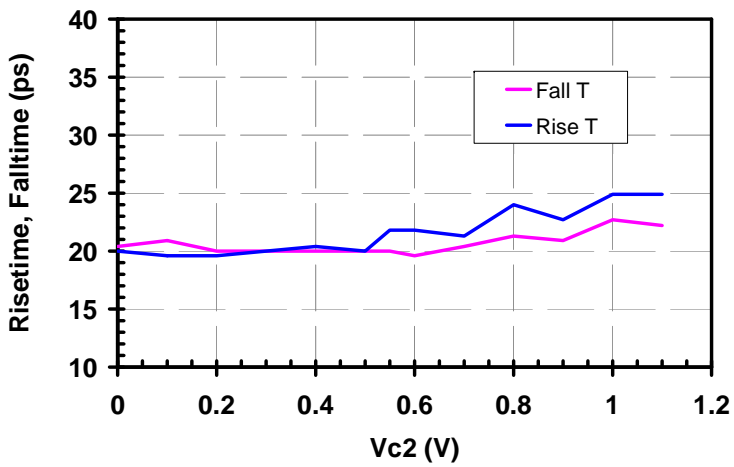
TGA4954-SL SN0635-001, 10.7 Gbps, 2^31-1 PRBS, RZ Input  
 Vin = 470 mVpp, 10.7 Gbps, Vd = 5V, Vc1=1V, Vg1=-0.76V, Vg2=0.12V



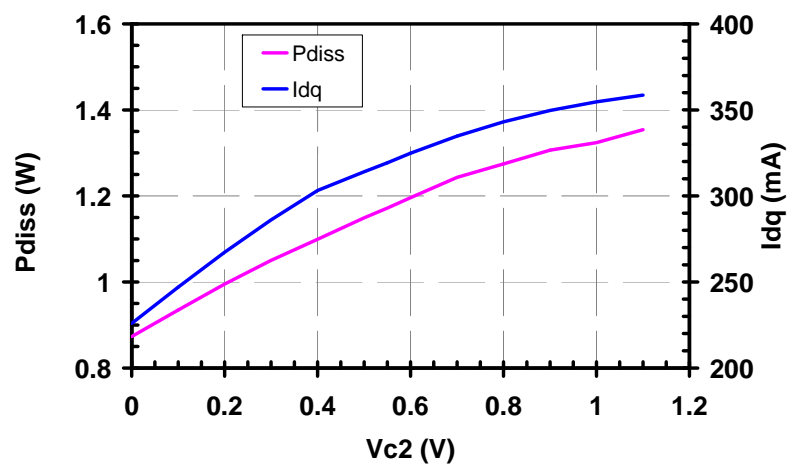
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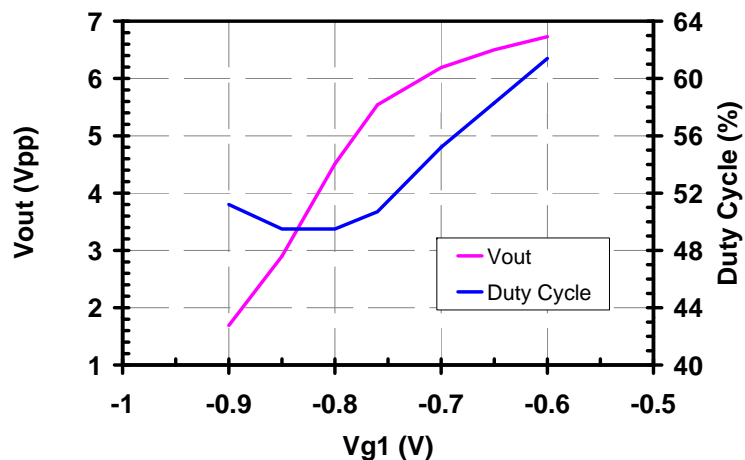


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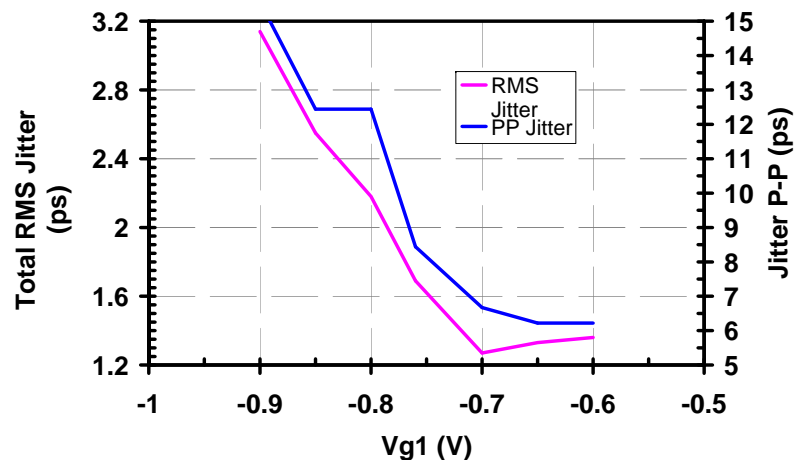


# Vary **Vg1** from initial conditions: **Vd = 5V, Vary Vg1, Vg2 = 0.12 V, Vc1 = 1.0 V, Vc2 = 0.55 V**

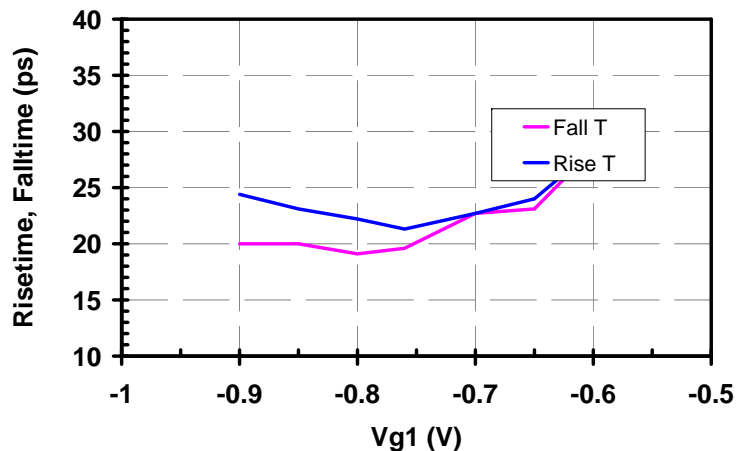
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 Vin = 470 mVpp, 10.7 Gbps, Vd = 5V, Vc1=1V, Vg2=+0.12V, Vc2=0.55V



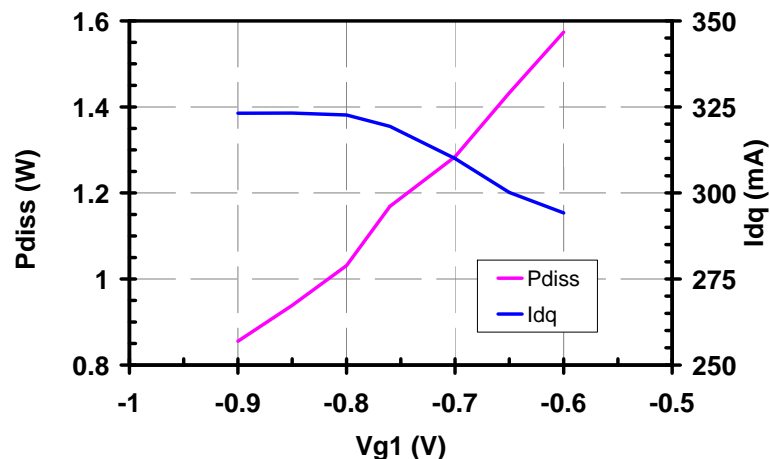
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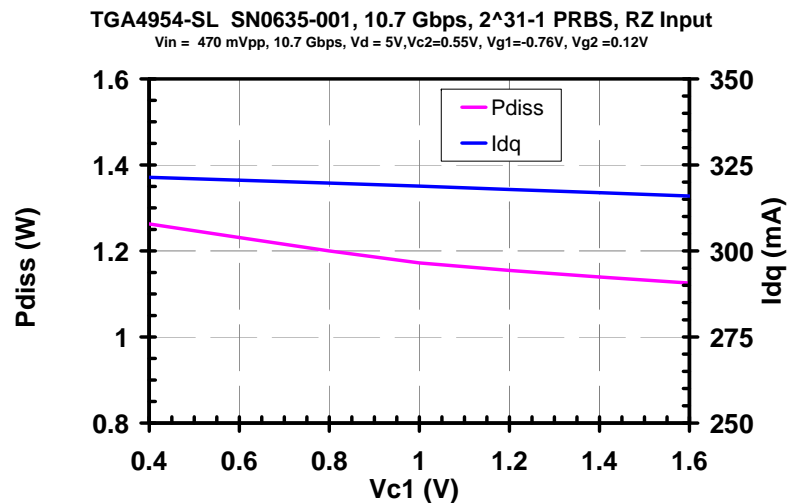
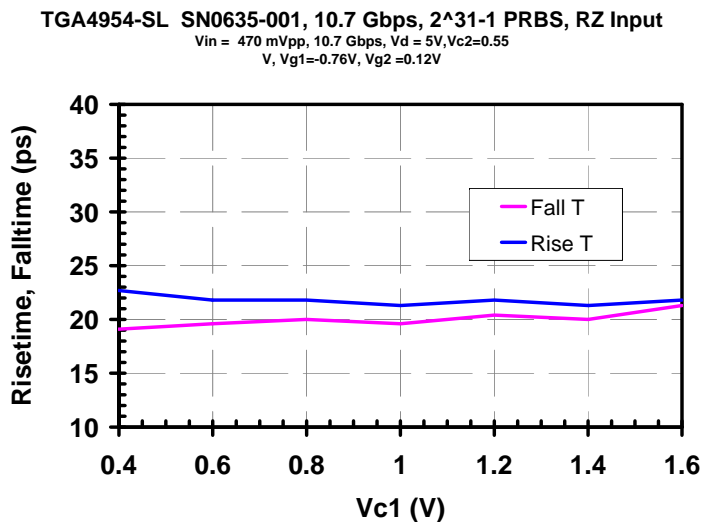
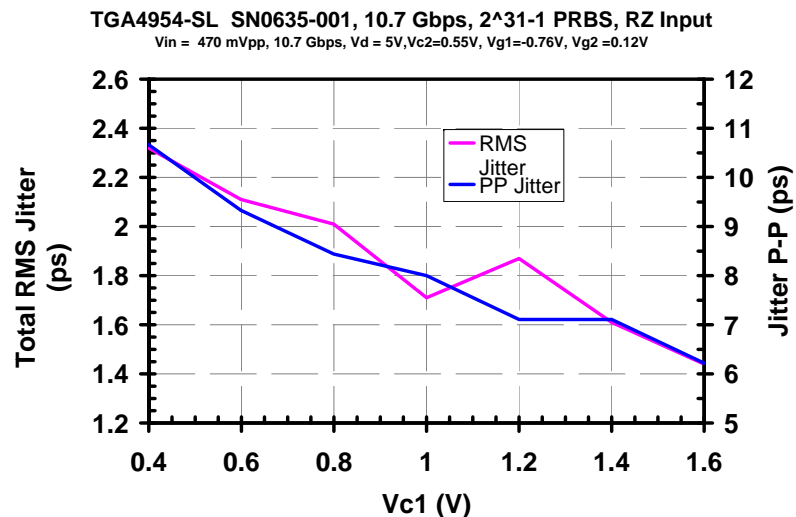
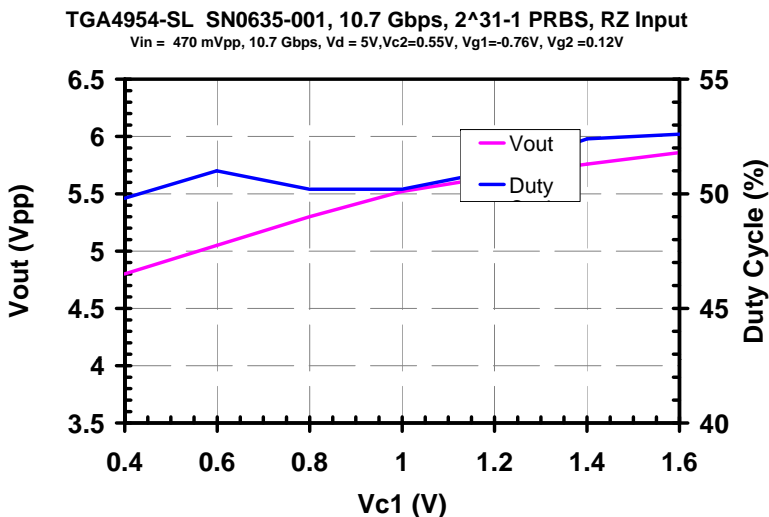
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 Vin = 470 mVpp, 10.7 Gbps, Vd = 5V, Vc1=1V, Vg2=+0.12V, Vc2=0.55V



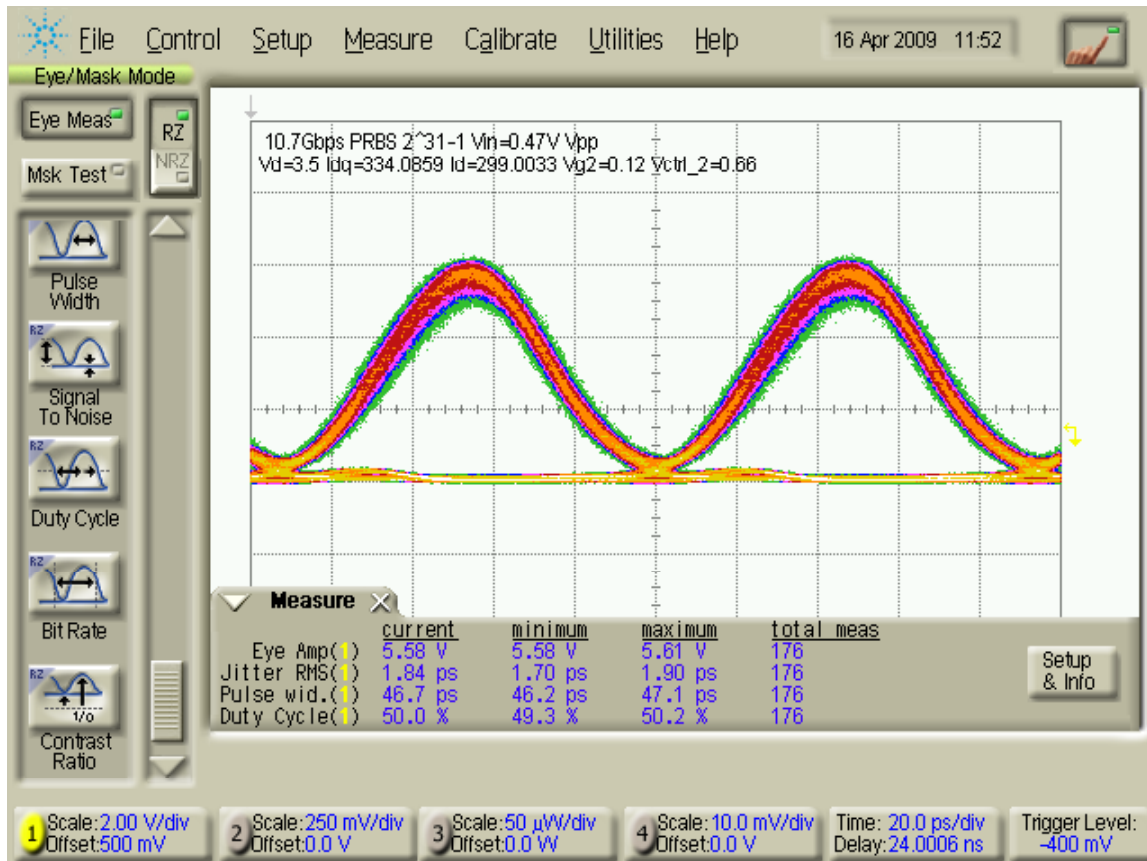
TGA4954-SL SN0635-001, 10.7 Gbps, 2<sup>31</sup>-1 PRBS, RZ Input  
 Vin = 470 mVpp, 10.7 Gbps, Vd = 5V, Vc1=1V, Vg2=+0.12V, Vc2=0.55V



# Vary **Vc1** from initial conditions: **Vd = 5V, Vg1 = -0.76V, Vg2 = 0.12 V, Vary Vc1, Vc2 = 0.55 V**



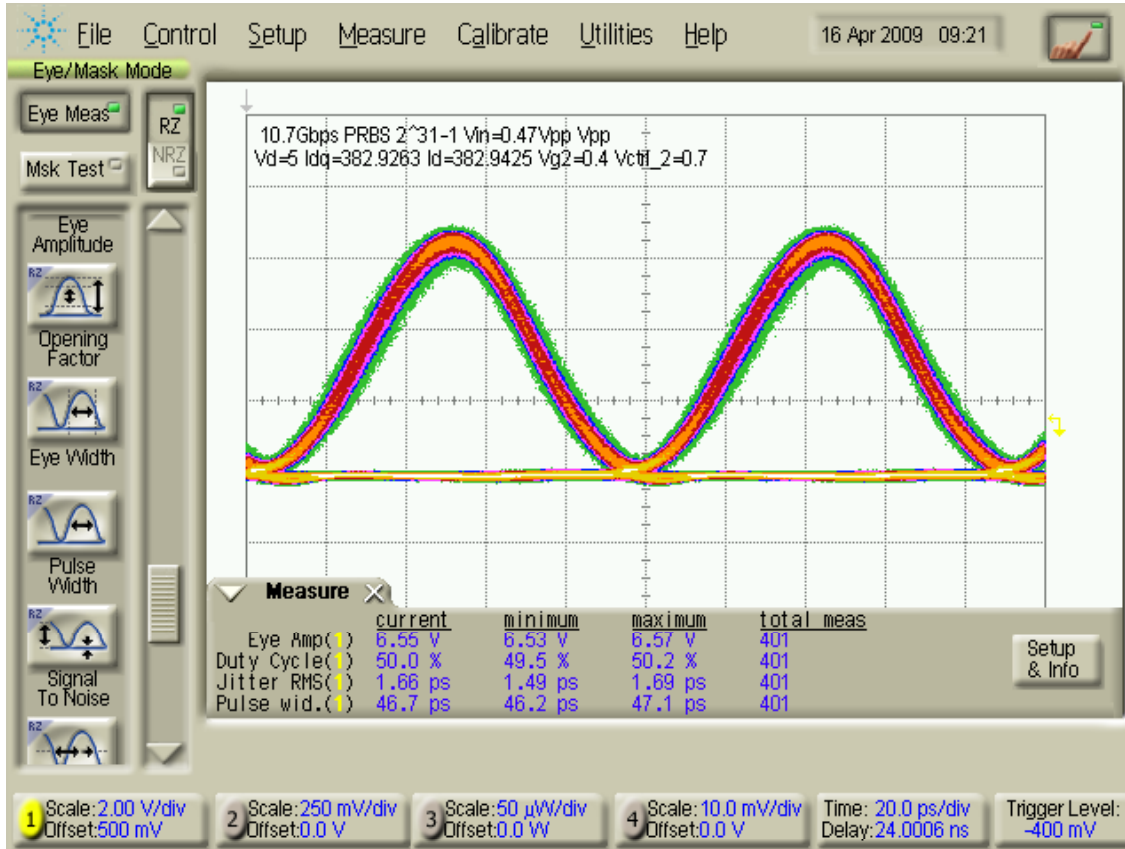
# Vout = 5.5 Vpp @ 50% Duty Cycle: **Reduce P<sub>diss</sub>**



- Data Rate = 10.7 Gbps
- Vout = 5.5 Vpp
- Duty Cycle = 50%
- Eye S/N = 17.7
- Rise, Fall T = 21, 21 ps
- **P<sub>diss</sub> = 0.74 W**

**Bias Conditions: V<sub>d</sub>=3.5V, I<sub>dq</sub> = 334 mA, V<sub>g1</sub> = -0.76 V, V<sub>g2</sub> = +0.12 V, V<sub>c1</sub> = 1 V, V<sub>c2</sub> = 0.66 V,**

# Vout = Max Vpp @ 50% Duty Cycle: Vd = 5 V



- Data Rate = 10.7 Gbps
- Vin = 0.47 Vpp
- Vout = 6.6 Vpp
- Duty Cycle = 50%
- Eye S/N = 12.7
- Rise, Fall T = 23, 20 ps
- **Pdiss = 1.6 W**

Bias Conditions: Vd=5 V, Idq = 400 mA, Vg1 = -0.73 V, Vg2 = +0.33 V, Vc1 = 1.4 V, Vc2 = 0.96 V,