

# Reliability Study of InGaP/GaAs HBT for 28V Operation

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**Abstract** — This paper reports the device process and reliability aspects of a high voltage InGaP/GaAs HBT technology for 28V operation. The key differences and challenges from the material and process perspectives relative to the conventional low voltage HBT technology are first described. Long-term reliability tests performed at 28V bias voltage, 5.2kA/cm<sup>2</sup> current density and 310°C junction temperature resulted in zero device failures after over 3600 hours of stress. Wafer-level reliability tests using extreme current stress conditions were used to force transistors to degrade in short time for quick checking of transistor integrity and process reliability. Transistor lifetimes were generally higher than those in conventional low voltage HBTs at similar junction temperatures. Combining with the previously reported ruggedness and linearity performance, the high voltage InGaP/GaAs HBT is a mature technology for use in the 28V high linearity power amplification.

**Keywords** – InGaP HBT; high voltage HBT; HBT reliability; wafer-level reliability.

## I. INTRODUCTION

InGaP/GaAs heterojunction bipolar transistors (HBTs) have widely been used in cellular phone handset and wireless infrastructure power amplifiers (PAs) because of their excellent linearity, reliability and efficiency. Typical operating voltage requirements in these applications are of the order of 3 to 7V. For base station applications with multi-watt output power requirements, higher operating voltages between 24 and 28V, and even up to 30V, are often needed. Because InGaP HBT has an intrinsic linearity advantage over other competing technologies and good reliability at low operating voltages, it would be very desirable if these intrinsic advantages can be extended to higher voltage operation.

Several groups have reported good reliability and good power performance of high voltage HBTs (HVHBTs) in the past several years [1–4]. In our previous work [5], we reported a state-of-the-art HVHBT technology that delivered high linearity and high efficiency power performance under high bias voltage operation of 24–28V. It exhibited P<sub>1dB</sub> of 8W under CW conditions, provided ACLR of –50dBc at 8.5dB power back-off and 16% efficiency under WCDMA signal (PAR = 8.7 dB) at 2.14GHz (test method 1). It sustained 10:1 output VSWR at 30V collector bias under P<sub>1dB</sub> driving conditions and over 6dB of gain compression

under the normal load impedance. In this work, we describe the device process and the reliability aspects of this technology.

## II. DEVICE AND PROCESS TECHNOLOGY

### A. Epitaxial Design

The basic emitter and base layer structures of the HVHBT are very similar to those of conventional InGaP/GaAs HBT operating at a lower voltage. In order to sustain the higher operating voltage required in multi-watt base station amplifier applications and to avoid triggering the Kirk effect and reaching the limit of the safe operating area (SOA), the collector layer structure in the HVHBT was carefully designed for optimal performance. The exact structure we used is proprietary, but a collector layer thickness of more than 3.0μm is generally needed to give a high enough base-collector breakdown voltage in excess of 60V. In addition, since the operating voltage is so much higher than those used in conventional HBT, the operating current density does not need to be as high as those in conventional HBT to deliver multi-watt output power. Therefore, the doping density in the collector structure of a HVHBT is generally lower than those in conventional HBTs. Furthermore, the collector structure must be designed such that the safe operating area (SOA) is not exceeded under large-signal and overdrive conditions [6]. Our optimized HVHBT exhibits BV<sub>cb0</sub> > 70V and BV<sub>ceo</sub> > 40V, and is capable of sustaining an operating current density of 5 kA/cm<sup>2</sup> and higher peak currents.

### B. Layout and Process Design

Since the emitter and base structures of the HVHBT are so much similar to those of conventional HBTs, the main differences in the fabrication process start from the base-collector mesa patterning and etching step. Due to the thick collector structure required for the high voltage operation, the finished HVHBT transistor is a highly non-planar structure. The design rules typically used for conventional HBTs were modified in such a way that sufficient room was made in the base-collector mesa dimension in layout to allow for larger lateral etching from the deep base-collector mesa etching and other layer patterns were biased smaller on top of the emitter and base contacts to accommodate for the thinner resist thicknesses on these high points of the wafer

surface. Device isolation was achieved through a combination of ion implantation and mesa etching.

The highly non-planar surface resulted after the completion of the base-collector mesa etching poses great challenge to all subsequent photolithography and liftoff processes. Overall resist coatings of at least as thick as the transistor mesa height were used to provide good step coverage over the tall transistor and diode mesa structures. In addition, the metal interconnection to emitter, base and collector contacts of transistors must also have good step coverage to prevent electromigration failures. The HVHBT process utilizes two frontside metal plating steps and three layers of polyimide coatings. The wafer thinning and backside processes were similar to those used in conventional HBTs. Figs. 1 and 2 show the FIB-SEM cross sections of the finished HVHBT as viewed from two different directions.

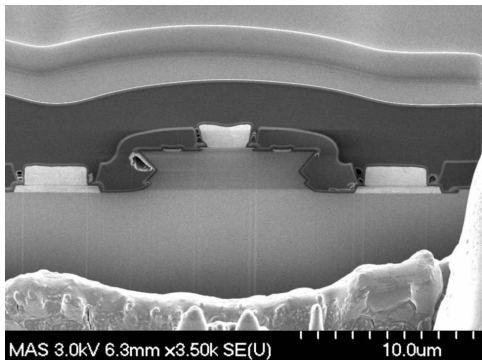


Figure 1. FIB-SEM cross section of a finished HVHBT as viewed from one direction.

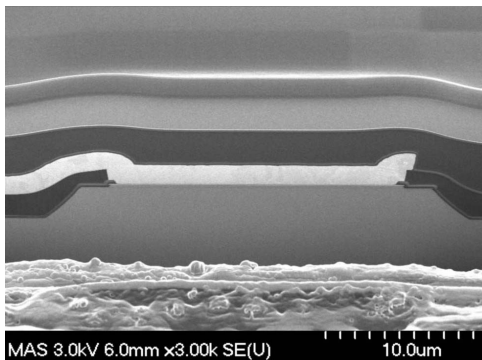


Figure 2. FIB-SEM cross section of a finished HVHBT as viewed from a direction perpendicular to the one used in Fig. 1 showing the M1 interconnection to the emitter contact of the transistor with good step coverage.

### C. Transistor Characteristics

The HVHBT had  $BV_{cbo} > 70V$  and  $BV_{ceo} > 40V$ . The  $I_c$ - $V_{ce}$  curves of a HVHBT with an emitter junction area of about  $1500\mu m^2$  are shown in Fig. 3. No thermal instability was observed in such a large transistor. The  $f_T$  and  $f_{max}$  of the basic HBT finger were 6.4 and 25GHz, respectively.

The device sustained 10:1 output VSWR at 30V collector bias under  $P_{1dB}$  driving conditions and over 6dB of gain compression under the normal load impedance as reported previously in [5].

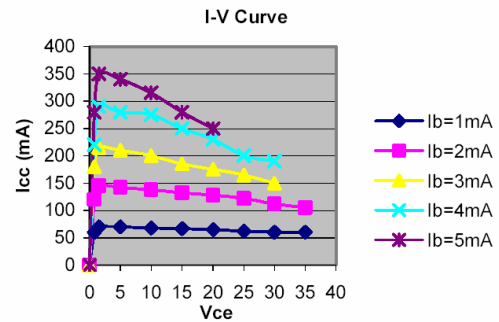


Figure 3. The  $I_c$ - $V_{ce}$  characteristics of an InGaP HVHBT with an emitter area of about  $1500\mu m^2$ .

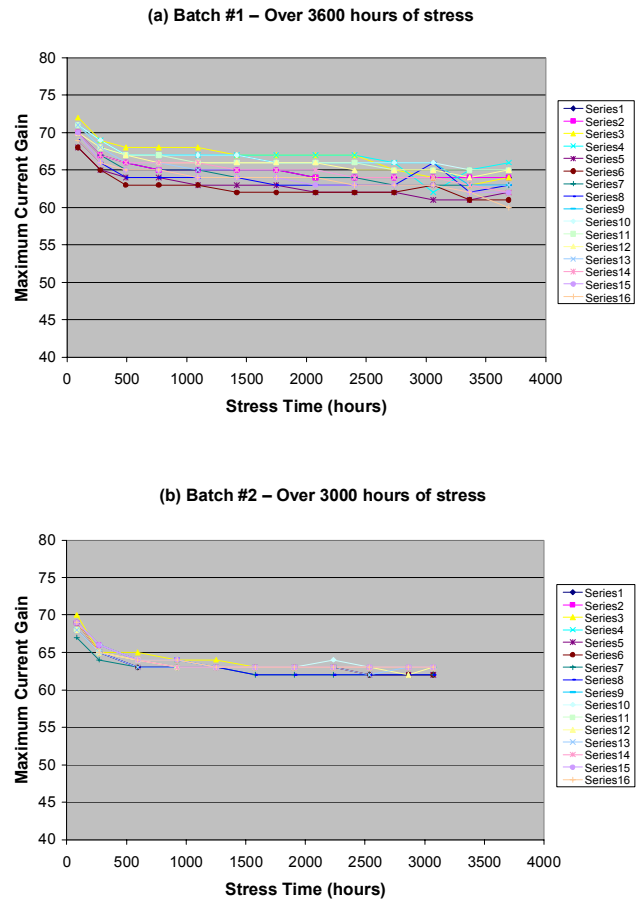


Figure 4. Interim life test results on two batches of HVHBTs with each transistor having a single finger emitter of size  $3 \times 8 \mu m^2$ . The transistors were stressed at 28V bias voltage and  $5.2kA/cm^2$  current density. The ambient temperature was  $230^\circ C$  and the junction temperature was  $310^\circ C$ . The maximum current gain was measured at room temperature.

### III. LONG-TERM RELIABILITY TESTS

Because of the use of high operating voltage, the operating current of a HVHBT is substantially lower than that of a conventional HBT for a similar output power. This can potentially result in longer lifetime since transistor degradation depends heavily on current density and not so much on bias voltage [4]. In order not to trigger any unwanted failure mechanisms caused by an extremely high junction temperature, we performed the long-term life tests of HVHBT at junction temperatures lower than 350 °C. Interim life test results on two batches of HVHBTs from two separate wafer lots with each transistor having a single emitter finger of size  $3 \times 8 \mu\text{m}^2$  are shown in Fig. 4. The ambient temperature was 230°C and the junction temperature was estimated to be 310°C. The collector bias voltage was 28V and the collector current was 1.25mA, which corresponds to a current density of  $5.2 \text{ kA/cm}^2$ . None of the 32 devices failed after the 3000+ hours of temperature and bias stress, and the MTTF has not yet been reached. The Gummel plots of a typical HVHBT before and after 3691 hours of stress are shown in Fig. 5. Little change in currents was observed.

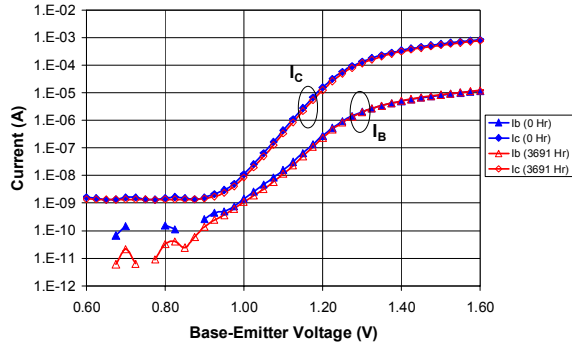


Figure 5. Gummel plots of a typical  $3 \times 8 \mu\text{m}^2$  HVHBT before and after 3691 hours of long-term stress at  $T_j = 310^\circ\text{C}$ ,  $V_{ce} = 28\text{V}$  and  $J_c = 5.2 \text{ kA/cm}^2$ .

### IV. WAFER-LEVEL RELIABILITY TESTS

Since the long-term life tests at high bias voltage and low current densities take thousands of hours to complete, wafer-level reliability (WLR) tests were also performed on the HVHBTs. The purpose of the WLR tests is not for

extracting the activation energy or predicting the MTTF of the devices under the normal “use” conditions, but for quick turnaround checking of the integrity and reliability of the transistors and fabrication process. The tests were done at much larger current densities than those typically used in long-term reliability life tests [7]. Extreme current densities were used to force devices to degrade in relatively short time. Degraded devices were then examined to see if a different failure mechanism other than the normal failure mode was triggered under these extreme bias stress conditions. The normal failure mechanism from WLR stress tests on conventional InGaP HBTs is the base current increase [7]. Other failure modes may indicate a weakness, a process or a material problem in the finished transistor.

In our test setup, transistor was put on a chuck at room temperature and stressed one at a time until the maximum current gain dropped below 30% of the initial value at room temperature. A junction temperature approaching 400°C or above was achieved solely from the device self-heating under the extreme bias stress conditions. Typical lifetimes of the HVHBTs and conventional HBTs under different WLR stress conditions are compared in Table I.

Typical changes in maximum current gain of a HVHBT upon the WLR stress are shown in Fig. 6. There was an initial rapid increase in current gain due to the filling of traps in the base layer by injected electrons, followed by a relatively fast decrease in current gain caused by H in the base layer being driven out upon the self-heating and bias, a relatively flat and stable region, and final degradation associated with an increase in base current as a result of defect generation. The corresponding Gummel plots of the same device before the WLR stress and right before the device failed are plotted in Fig. 7.

Fig. 8 compares the HVHBT and conventional HBT lifetimes obtained from the WLR tests. Due to the differences in current acceleration factor in the life tests, the onset of Kirk effect and current handling capability as a result of the differences in collector doping concentration, it is difficult to draw to a conclusion on which device type is more reliable they are designed and targeted for different operating conditions. Nevertheless, because a HVHBT operates at a lower current density than a conventional HBT, its lifetime appears to be much longer for a given junction temperature.

TABLE I. Lifetimes of Conventional and High Voltage InGaP HBTs of  $3 \times 4 \mu\text{m}^2$  emitter areas biased at different WLR stress conditions.

Technology	Device	$I_c$	$V_{ce}$	$I_b$	Current Density	Power Density	$T_j$	Lifetime
Conventional HBTs	A	52.8mA	2.3V	1.00mA	440 $\text{kA/cm}^2$	1.02 $\text{MW/cm}^2$	396°C	101 Hrs
	B	60.1mA	2.0V	1.30mA	501 $\text{kA/cm}^2$	1.02 $\text{MW/cm}^2$	394°C	17 Hrs
	C	58.0mA	2.3V	1.50mA	483 $\text{kA/cm}^2$	1.13 $\text{MW/cm}^2$	433°C	10 Hrs
HVHBTs	A	4.7mA	29.1V	0.13mA	39 $\text{kA/cm}^2$	1.14 $\text{MW/cm}^2$	435°C	305 Hrs
	B	4.7mA	28.4V	0.14mA	39 $\text{kA/cm}^2$	1.12 $\text{MW/cm}^2$	428°C	161 Hrs
	C	9.4mA	15.1V	0.20mA	78 $\text{kA/cm}^2$	1.18 $\text{MW/cm}^2$	449°C	17 Hrs
	D	35.2mA	3.5V	1.50mA	293 $\text{kA/cm}^2$	1.06 $\text{MW/cm}^2$	406°C	28 Hrs
	E	33.3mA	4.4V	1.50mA	278 $\text{kA/cm}^2$	1.26 $\text{MW/cm}^2$	480°C	49 Hrs

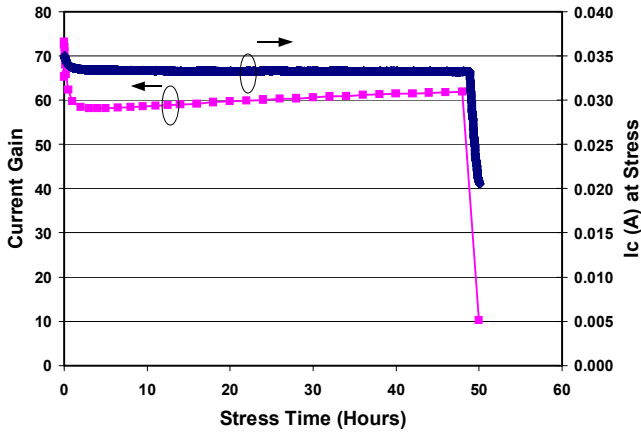


Figure 6. Typical degradation behavior of a  $3 \times 4 \mu\text{m}^2$  HVHBT under WLR stress. The bias conditions were:  $V_c = 4.44\text{V}$ ,  $V_b = 2.5\text{V}$ ,  $I_c = 33.3\text{mA}$  ( $J_c = 278 \text{ kA/cm}^2$ ),  $I_b = 1.5\text{mA}$ , and  $P_{\text{diss}} = 151.6\text{mW}$ . The estimated  $T_j = 480^\circ\text{C}$ .

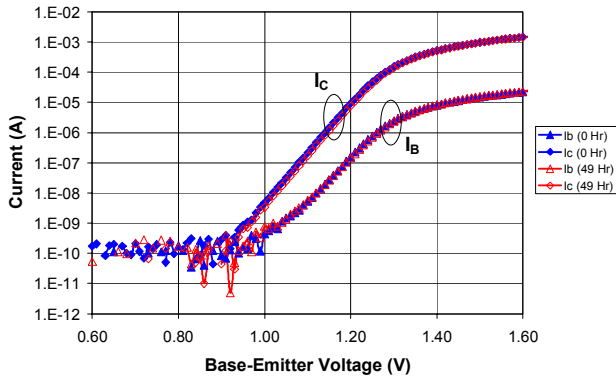


Figure 7. Gummel plots of the same HVHBT in Fig. 6 before the WLR stress and right before the device failed.

## V. SUMMARY

We have demonstrated a high voltage InGaP/GaAs HBT technology with  $BV_{\text{cbo}} > 70\text{V}$  and  $BV_{\text{ceo}} > 40\text{V}$ . The key differences and challenges in the HVHBT process were briefly outlined from the material and process perspectives. No transistor failures were observed after over 3600 hours of stress at  $V_{\text{ce}} = 28\text{V}$ ,  $J_c = 5.2\text{kA/cm}^2$  and  $T_j = 310^\circ\text{C}$ . Wafer-level reliability tests using extreme current stress for quick turnaround checking of the transistor and process integrity showed that the HVHBTs had generally longer lifetimes than the conventional low voltage HBTs at similar junction temperatures. It is perhaps related to the low target operating

current densities in the HVHBTs as reported in [4]. Combining with the previously reported ruggedness and linearity performance of the same technology [5], the high voltage InGaP/GaAs HBT is a mature technology for use in the 28V high linearity power amplification.

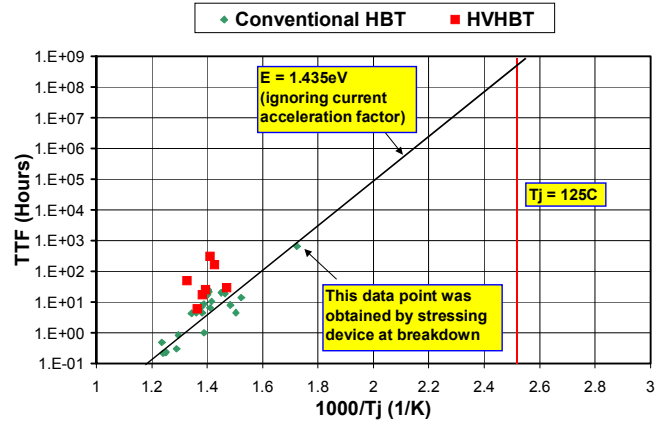


Figure 8. Comparison of WLR test results between HVHBTs and conventional HBTs.

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