

28V High-Linearity and Rugged InGaP/GaAs Power HBT

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Abstract — This paper reports on the improvement of a previously developed InGaP/GaAs HBT for 24-28V linear power operation. The improvements achieved were: application of dynamic bias circuit which improves the ACLR under WCDMA modulation; modification of device technology improving ruggedness to sustain 10:1 VSWR at 30V collector bias under P_{1dB} driving conditions and over 6 dB of gain compression; maintenance of lifetime and reliability simultaneously. Building blocks of HBT were strung together for higher power and good scaling of performance was achieved supporting the validity of the layout approach and the thermal design. Devices delivering $P_{1dB} = 8W$ under CW conditions provided ACLR = -50 dBc at 8.5 dB back-off and 16% efficiency for WCDMA signal (PAR=8.7 dB) at 2.14 GHz. Lifetime test over 3000 hours was repeated for 28V bias and $0.05mA/\mu m^2$ current density at 315 degree C junction temperature. Therefore, the InGaP/GaAs HBT technology is mature now for the high linearity power amplification.

Index Terms — Heterojunction bipolar transistor, power bipolar amplifiers, interchannel interference, power amplifiers.

I. INTRODUCTION

InGaP/GaAs HBT has become the dominant technology for handset power amplifier application with its linearity and efficiency. The suitability of InGaP/GaAs HBT for power amplifier in base station market has been explored. The base station PA application requires operation at high voltages: 24V to 28V and even above 30V. An InGaP/GaAs HBT technology was developed previously in our labs for 28V power amplification applications [1,2], which is compatible with standard MMIC technology.

The high breakdown voltage of the HBT was achieved with a thicker collector. Multiple fingers are arranged into a single building block with emitter area around $1500 \mu m^2$. Multiple building blocks can be arrayed into a large size power HBT; each building block can deliver 2W RF power in the 1-3GHz band. The f_T and f_{max} of the basic HBT finger are 6.4GHz/25GHz respectively.

Excellent result was reported earlier [1,2,3]. It was also reported that matching circuit with low source impedance at the modulation frequency improves the linearity in the class AB operation [2,4]. In a typical lineup of power amplifier chain, the power stage is often a class B circuit for the best efficiency, and the driver stage a class AB for a tradeoff of linearity and efficiency, and pre-driver stage may be a class A. In this effort, the goal is to operate the driver and pre-driver stages in near class B operation for better efficiency, while

achieving a superior linearity at the back-off power level. This is achieved with a dynamic bias circuit and the fine adjustment of the emitter ballasting. In addition the ruggedness is improved to withstand high output mismatch of 10:1 VSWR with typical input power at 1dB gain compression and over-drive condition of typical 8dB gain compression into 50 ohm load at 30V.

II. POWER HBT DESIGN

The 28V HBT device structure is the same as the standard 3-5V HBT except a much thicker collector layer. To sustain peak voltage over 60V, a collector thickness of 3 microns is required.

Safe operation area (SOA) of the HBT is limited by several factors. The thermal SOA was designed by adjusting the thermal resistance (through layout) and the ballasting [1]. The breakdown voltage of the HBT must be higher than 28V with margin; therefore BV_{ceo} is chosen to be about 35V and BV_{cbo} is over 70V [5]. The load contour of the bipolar transistor can swing beyond the BV_{ceo} without any negative impact to performance or reliability, since the source impedance (presented to the base) is not matched by an “open circuit” in the real circuitry.

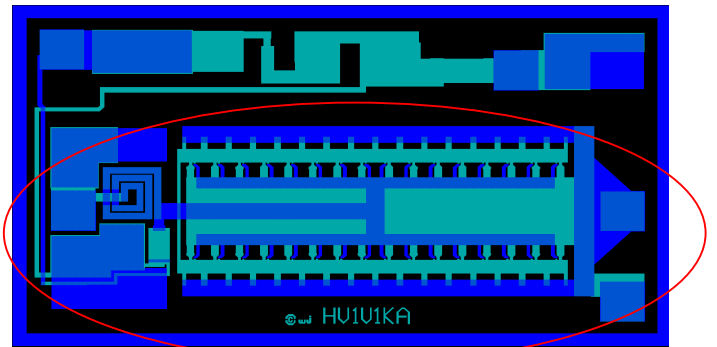


Fig. 1. Schematic layout for 1BB device containing $(3 \times 20) \mu m^2 \times 32$ fingers. The building block and the pre-matching circuit are circled out.

The power HBT is laid out in the building block approach. Figure 1 shows the layout of a single building block with the bias circuit. Higher power can be achieved by arraying building blocks in parallel. Electromagnetic simulation tool is used to make sure the individual HBT fingers in the building

blocks will have equal amplitude and phase at the desired operation frequency. At higher frequencies, the RF power is no longer evenly distributed among the HBT fingers degrading the device performance.

Multi building blocks structure was also designed with the electromagnetic simulation. The input impedance is raised to facilitate the matching by an on-chip pre-match circuit. The higher input impedance also improves the RF signal uniformity across the building blocks. Each building block has its own bond wire connection to the pins of the package.

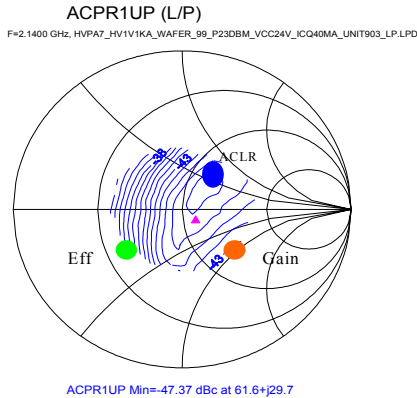


Fig 2- Optimization "triangle" obtained from Load Pull with constant output power.

The device was eutectic mounted into a ceramic package, and the package is surface mounted onto the evaluation circuit board. The evaluation board was submitted to load pull with constant output power for matching impedance optimization. The load pull result of the 50Ω matched amplifier is shown. For simplicity, only the ACLR contours are shown on figure 2, along with the impedance points for best gain and efficiency. It clearly shows that the gain, efficiency, and the linearity (in ACLR) each has a respective sweet spot in the Smith Chart.

The optimal load impedance of $Z_{load} = 16.8 + j45\Omega$ at the HBT collector, corresponds to $R_L = 136\Omega$ in parallel with a shunt inductive impedance which resonates with a 1.45pF output capacitance, complying with the class AB operation of the power HBT with a C_{bc} around 0.6pF. The 2nd harmonic load impedance is shorted.

III. LINEARITY IMPROVEMENT

The driver stage for power amplifier chain is often biased toward class A in order to provide the needed linearity. This approach sacrifices the operation efficiency. In the past, a low frequency low source impedance matching was found to improve the linearity in near class B operation [2]. However there is certain constraint on the range of the emitter resistance value. In this paper, a dynamic bias circuit is used to allow the simultaneous achievement of high linearity and near class

B efficiency, while removing the constraint on the range of the emitter resistor.

The major non-linearity in the bipolar transistor is found to come from the exponential I-V relationship. Following the previously reported analysis [6], HBT is found to have similar behavior as LDMOS in the 3rd order derivative of the $I_c(V_{in})$ as shown in Figure 3.

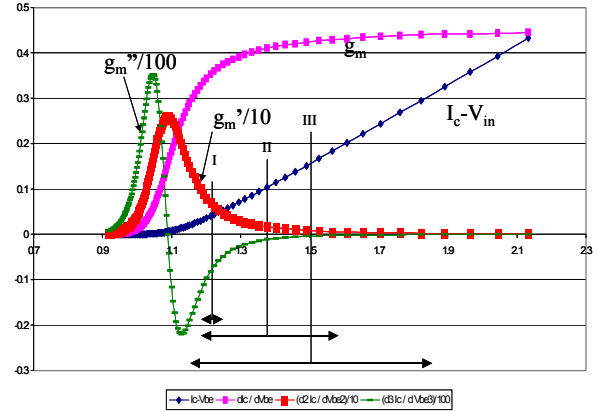


Fig 3- Analysis of the 3rd order intermodulation distortion contributed by the transconductance nonlinearity in bipolar transistor

The curve of $I_c - V_{in}$ along the load line follows the exponential relationship with the ballasting resistor effect. The quiescent bias point is at point I. For conventional Class B operation, the DC average voltage will remain at point I regardless of the RF swing. With the dynamic bias circuit, the time average bias point is lifted up to conditions II then III as the input power level is increased. The RF voltage avoids swinging into the peaking portion of the $g_m''(V_{in})$ curve as the bias point is lifted by the dynamic bias circuit; thus improving the linearity in near class B operation.

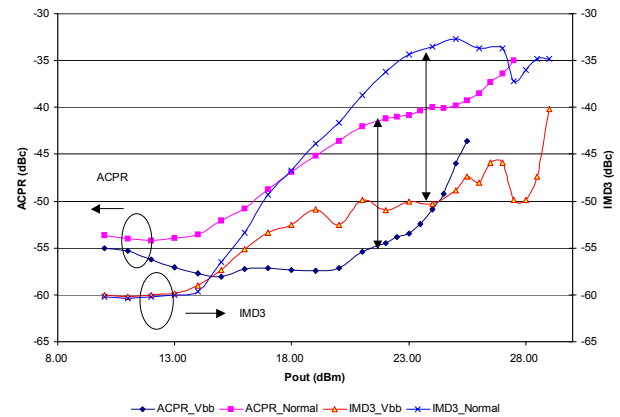


Fig 4- Comparison of linearity with and without the dynamic bias circuit.

Figure 4 compares the 1BB power HBT (with $P_{sat} \sim 33\text{dBm}$) tested under two-tone and WCDMA signals at 2.14GHz with

and without the dynamic bias circuit in the near class B bias condition. The improvement of the linearity by the dynamic bias circuit is most noticeable over the output power range within 15 dB of the P_{1dB} . At 20dBm average P_{out} , the ACLR of WCDMA signal improves over 10dB. The IM3 improves by 15dB at 23dBm output power.

IV. LINEARITY PERFORMANCE

The high linearity performance scales well and the ruggedness is maintained with the size of HBT up to 4 building blocks (about 8W P_{1dB}). This proves that the basic power transistor design/layout is sound and maintains equal phase and magnitude of RF signal over every HBT finger.

The amplifiers of 1, 2 and 4 building blocks were matched and tested first by a CW signal and the result is shown in figure 5. The power level scales well with the size of the power HBT, and the efficiency is maintained over the size. Efficiency near 50% is achieved at 1dB gain compression point for HBTs of all three sizes. The frequency response achieves less than 1 dB gain variation over the 2.11 to 2.17 GHz band.

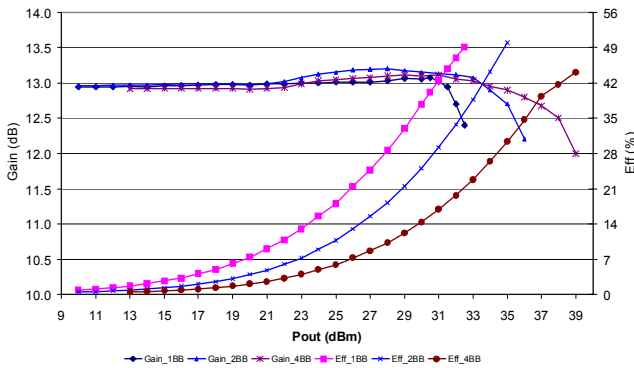


Fig 5- Gain and Efficiency versus output power for: 1BB, 2BB and 4 BB. Signal is CW waveform at 2.14 GHz.

Then the amplifier was submitted to a WCDMA signal with PAR = 8.7 dB at the center frequency of 2.14 GHz. The ACLR performance for all 3 building blocks is exhibited in figure 6.

Observe that ACLR = -50 dBc is achieved with 8.5 dB power back-off. The efficiency at this point is 16% for all 3 sizes HBT. The ACLR quickly improves to -55 dBc with further power back-off. At high average power (with peak power beyond the P_{sat} level), the peak power is clipped and ACLR degrades rapidly. When P_{ave} is below P_{sat} -PAR, the linearity is determined by the transistor and the circuitry; here the dynamic bias circuit greatly improves the linearity in the near class B bias operation. Compared with previous

technology [1], more than 10 dB improvement in ACLR was obtained.

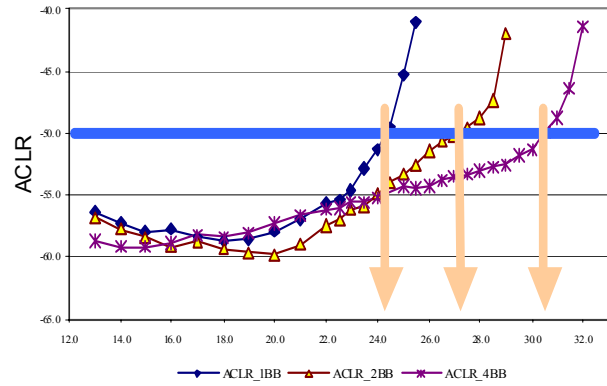


Figure 6 - Comparison of ACLR versus output power for 1BB, 2BB and 4BB. Signal is WCDMA waveform at 2.14 GHz

The power HBT with dynamic bias circuit also performs well on other modulation schemes. For instance, submitting the 2BB test amplifier to a CDMA2000 waveform at PAR = 8.7dB with 9 forward channels, operating under the same carrier frequency, resulted in ACLR = -45 dBc at P_{out} = 30.5 dBm.

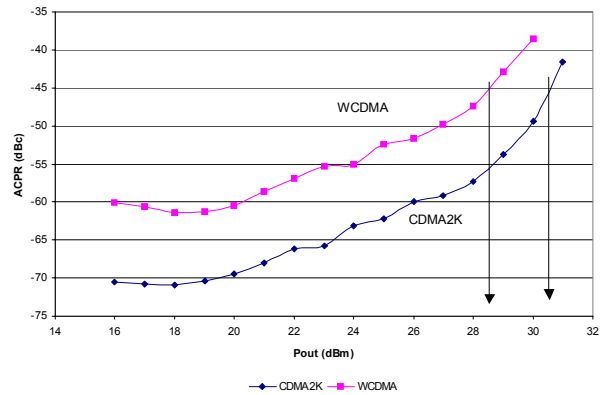


Figure 7 - Comparison of ACLR/ACPR under different modulation signals for the same power HBT

The dynamic bias circuit demonstrated excellent temperature stability as evaluated over the -40 to +85°C range. A 2BB size HBT with the dynamic bias circuit was evaluated over temperature with its result shown in figure 8. At ACLR=-50dBc under WCDMA signal, the output power is maintained within 1dB; the efficiency at ACLR=-50dBc is 16% over the same temperature range.

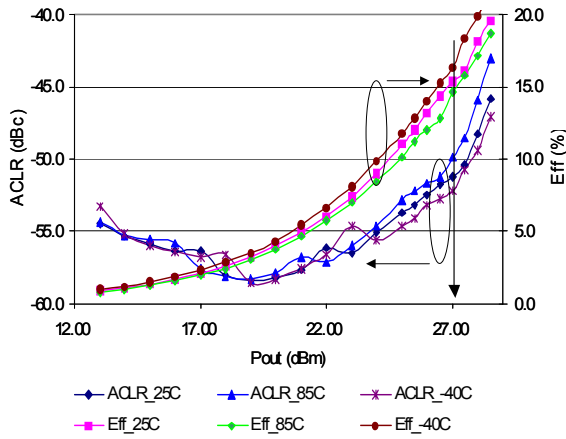


Fig 8 - ACLR and Efficiency versus Temperature for 2BB.

V. RUGGEDNESS AND RELIABILITY

The power device, under normal usage, may be subjected to mismatch or over-drive condition and it must be rugged enough to survive such condition. The ruggedness is related to the level of ballasting. Under the presently chosen ballasting level, the three HBTs of 1BB, 2BB and 4BB were individually tested for output mismatch. The input power is held constant at the level providing output power of P_{1dB} under normal operation; then the output load is changed from 50 ohms to 10:1 under all phases. The test started at $V_{cc} = 24V$ and went all the way up to 30V without any observed device degradation.

With the PAR (peak-to-average ratio) of the modulation signal in the 6 to 10dB range, it is not uncommon to have the peak power level overdrive the amplifier beyond the 1dB gain compression point. Therefore another test was conducted with the RF over-drive under the normal matching condition with collector biased at 28V. For all three sizes, 8dB gain compression at 2.14GHz was achieved without damage or degradation with the SINE wave CW signal.

The improvement in linearity and robustness is achieved without any loss of the lifetime and reliability of the transistor technology. Several rounds of accelerated lifetime were conducted. At 28V bias and $0.05 \text{ mA}/\mu\text{m}^2$ quiescent bias current, 3000 hours test were repeated (and still on going) at junction temperature of 310 °C. This level of lifetime is expected as 28V HBT operates at lower current density than its 5V counterpart, and the high current density is one key factor to the long lifetime operation. The collector sidewall in 28V HBT has not shown any leakage in the accelerated lifetime test. These tests demonstrate that 28V HBT not only maintains the same level of lifetime as the 5V InGaP/GaAs HBT, but also is rugged against mismatch, RF power overdrive, and V_{cc} fluctuations.

VII. Conclusion

Excellent linearity and efficiency in 28V power HBT is achieved with the dynamic bias circuit. The combination of the high linearity RF performance in the back-off power level, the ruggedness in RF power overdrive and the output mismatch condition, and the long lifetime, demonstrated that InGaP/GaAs HBT technology is mature to serve the 28V linear power operation in infrastructure market.

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