



**0.5  $\mu\text{m}$  pHEMT Device Cross-Section**

## General Description

TriQuint's TQPED process is based on our production-released 0.5  $\mu\text{m}$  TQPHT process. TQPED partners an E-Mode pHEMT device with our TQPHT D-Mode transistors to be the first foundry pHEMT process to integrate E-Mode and D-Mode transistors on the same wafer. This process is targeted for low noise amplifiers, linear, low loss and high isolation RF switch applications, converters and integrated RF Front Ends. The TQPED process offers a D-Mode pHEMT with a  $-0.8\text{ V}$  pinch off, and an E-Mode pHEMT with a  $+0.35\text{ V}$  threshold voltage. The three metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost-effective die sizes.

## Features

- E-Mode, 0.35 V,  $V_{th}$
- D-Mode,  $-0.8\text{ V } V_p$
- InGaAs Active Layer pHEMT Process
- 0.5  $\mu\text{m}$  Optical Lithography Gates
- High Density Interconnects:
  - 2 Global
  - 1 Local
- High-Q Passives
- Thin Film Resistors
- High Value Capacitors
- Backside Vias Optional
- Based on Production TQPHT pHEMT and Interconnect
- Nominal TOM3 FET Models Available

## Applications

- Highly Efficient, and Linear Power Amplifiers
- Low Loss, High Isolation, Low-Harmonic Content Switches
- Integrated digital control logic for Switches and Transceivers
- Converters
- Integrated RF Front Ends— LNA, SW, PA
- Wireless Transceivers, Base stations, Direct Broadcast Satellite Radars, Digital Radios, RF / Mixed Signal ICs
- Power Detectors and Couplers

**TQPED  
Process  
Details**
**Process Details @  $V_{ds} = 3.0V$** 

Element	Parameter	Value	Units	
D-Mode pHEMT	$V_p$ (1 $\mu A/\mu m$ )	-0.8	V	
	$I_{dss}$ (3V)	230	mA/mm	
	$I_{max}$ (3V)	515	mA/mm	
	Breakdown, $V_{dg}$	15 min, 20 typ	V	
	$f_t$ @ 50% $I_{dss}$	27	GHz	
	$f_{max}$ @ 50% $I_{dss}$	90	GHz	
	$G_m$ (50% $I_{dss}$ )	365	mS/mm	
	$R_{on}$	1.4	Ohms * mm	
	E-Mode pHEMT	$V_{th}$ (1 $\mu A/\mu m$ )	+0.35	V
		$I_{dss}$	0.1	$\mu A/\mu m$
$I_{max}$		320	mA/mm	
Breakdown, $V_{dg}$		15 min, 18 typ	V	
$f_t$ @ 50% $I_{dss}$		33	GHz	
$f_{max}$ @ 50% $I_{dss}$		100	GHz	
$G_m$ (50% $I_{dss}$ )		600	mS/mm	
$R_{on}$		2.5	Ohms * mm	

**Common Process Element Details**

Gate Length		0.5	$\mu m$
Interconnect		3	Metal Layers
MIM Caps	Value	630	pF/mm <sup>2</sup>
Resistors	NiCr	50	Ohms/sq
	Bulk	320	Ohms/sq

**Maximum  
Ratings**

Storage Temperature Range	-65 to +150	Deg C
Operating Temperature Range	-55 to +150	Deg C
EFET/DFET Transistor ( $V_s$ open; $I_{dg} = 1 \mu A/\mu m$ )	15	V
Capacitor	40	V



# TQPED

## 0.5 um E/D pHEMT Foundry Service

### Prototyping and Development

- Prototype Development Quick Turn (PDQ):
  - Shared mask set
  - Run monthly
  - Hot Lot cycle time
- Prototype Wafer Option (PWO):
  - Customer-specific masks; Customer schedule
  - 2 wafers delivered
  - Hot Lot cycle time
  - With thinning and sawing; optional backside vias

### Process Qualification Status

- Mature process based on TQPHT 150-mm process
- Process fully released to production
- Full 150mm wafer Process Qualification complete
- For more information on Quality and Reliability, contact TriQuint or visit: [www.triquint.com/manufacturing/QR/](http://www.triquint.com/manufacturing/QR/)

### Design Tool Status

- Complete Design Manual Now
- Device Library of circuit elements: FETs, diodes, thin film resistors, capacitors, inductors
- Design Kit for Agilent's ADS design environment
- Design Kit planned for AWR Microwave Office
- Layout Library in GDS II format
- Cadence Development Kit with PCells in Preliminary Release
- Layout Rule Sets for Design Rule Check for ICED, Cadence
- Qualified package models for supported package styles
- Noise parameters on specific device sizes available

### Applications Support Services

- Tiling of GDSII stream files including PCM
- Design Rule Check services
- Layout Versus Schematic check services
- Packaging Development Engineering
- Test Development Engineering:
  - On-wafer
  - Packaged parts
- Thermal Analysis Engineering
- Yield Enhancement Engineering
- Part Qualification Services
- Failure Analysis

### Training

- GaAs Design Classes:
  - Half-Day Introduction; Upon request
  - Four-Day Technical Training; Fall and Spring at TriQuint Oregon facility
- For Training & PDQ Schedules, please visit: [www.triquint.com/foundry/](http://www.triquint.com/foundry/)

### Manufacturing Services

- Mask making
- Production 150-mm wafer fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Diesort Testing
- RF On-wafer testing
- Plastic Packaging
- RF Packaged Part Testing

**Please contact your local TriQuint Semiconductor Representative/ Distributor or Foundry Services Division for Additional information:**  
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